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QUARTERLY REPORT NO. 4

PRODUCTION ENGINEERING MEASURE
ON
2N1708 SILICON PLANAR EPITAXIAL TRANSISTOR

CONTRACT NO. DA-36-039-SC-86729

FOR

U.S. ARMY ELECTRONICS MATERIEL AGENCY
PHILADELPHIA, PENNSYLVANIA

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use of an encapsulant. When devices were evaluated on operating life, however, it was found that better results were obtained on devices without an encapsulant. To increase operating life performance an improved encapsulant has been incorporated into the standard process.

Production problems which developed on the ceramic stem have been minimized. It has been decided that it is not to the best interests of the program to begin to evaluate this stem in terms of the reliability goals of the contract. The reliability goals will be achieved by the glass to metal stem developed earlier in the program.

Inspection and Quality Control

A Quality Control and Inspection Plan was submitted to the Signal Corps on 24 April 1963.

Reliability Testing and Analysis

The use of high temperature shelf life tests to permit rapid evaluation of process changes and to determine acceleration factors is discussed. The use of Weibull probability paper to establish the cumulative percent failures versus time is demonstrated. Extrapolation of mean failure time versus 1/T is used to obtain failure distributions at other than test temperatures. Acceleration curves are developed.

An evaluation of methods of measurement of thermal resistance is presented. The variation of junction temperature due to the following effects is discussed.

a. Ambient conditions-particularly in regard to the movement of air. Data on the variation of thermal resistance with power dissipation is provided.

b. Life test circuit and transistor parameters.

A study of failure rates was made on devices similar to the 2N1708.

Graphs are presented showing the instantaneous failure rate variation with time on shelf and operating life tests.

The results of a study of the effect of variations at V_{CB}=15, 12 and 6 volts on 300 mw operating life tests are presented.

A study of the effect of 300°C temperature aging on 300 mw, 25°C operating life tests was performed. A review of the results of several tests is presented.

A discussion of the use of variables data on accelerated life tests to evaluate the stability of individual units and distributions is given. Examples of the value of this type of analysis in this program are provided.

The use of power step stress tests to evaluate process changes is reviewed. The advantages and limitations as demonstrated by tests performed on this program are discussed.

I. PURPOSE

The objective of this contract is to improve the reliability of the RCA 2N1708 (TA2100A) epitaxial, planar, silicon switching transistor. The failure rate goal, at a 90 percent confidence level, is 0.0011 percent per thousand hours at a junction temperature of 25°C.

To attain this objective, design and process improvements will be evaluated and put into effect. A system of process controls will be established.

Various reliability tests will be performed. These will include: step stress tests; matrix tests; temperature and/or power aging tests; life tests; and mechanical and environmental tests.

A 9 to 12 month development period followed by a 6 month production phase will be undertaken. During this latter period, life testing will be employed to establish the actual failure rate of the improved 2N1708.

II. DELIVERY OF ENGINEERING SAMPLES

State-of-the-art samples were shipped to the U. S. Army Electronics Research and Development Laboratory as indicated below:

NUMBER	DATE OF SHIPMENT
12	1 June 1962
12	15 August 1962
12	1 November 1962
12	1 March 1963

The electrical characteristics of the 12 samples shipped 1 March 1963 are shown in Table I. The electrical characteristics shipped 1 June 1962 were provided in Quarterly Report No. 1, the 12 samples shipped 15 August 1962 were provided in Quarterly Report No. 2 and the 12 samples shipped 1 November 1962 were provided in Quarterly Report No. 3. The 2N1708 Electrical Specifications are shown in Table II.

TABLE I

RCA 2N1708 STATE-OF-THE-ART SAMPLES, 1 MARCH 1963

Unit No.	Shell Code No.	I_{CBO} 25°C μa	I_{CBO} 150°C μa	BV_{CBO} v	BV_{EBO} v	BV_{CEO} v	V_{BE} 10ma v	V_{CE} 10ma v	V_{CE} 50ma v	C_{OB} pf	h_{FE} 10ma	h_{fe} 100mc	T_S nsec	T_{ON} nsec	T_{OFF} nsec
1	CCH	.0032	03.7	58.7	7.24	21.1	.732	.142	.200	04.5	72.0	4.25	12.0	19.5	40.0
3	CEB	.0031	03.5	59.4	7.55	21.6	.738	.149	.221	04.5	60.0	4.00	11.5	19.5	40.0
5	CBK	.0032	03.7	61.8	6.95	21.1	.734	.143	.210	04.5	80.0	4.18	12.5	19.0	40.0
7	CCG	.0024	03.1	60.5	6.78	22.1	.740	.151	.226	04.7	50.0	3.95	11.0	20.0	38.0
10	BFE	.0029	03.0	60.6	7.47	21.9	.743	.151	.227	04.5	52.0	4.00	12.0	20.0	40.0
12	CAK	.0052	05.4	61.1	7.10	22.0	.737	.153	.221	04.5	52.0	4.05	10.5	19.8	36.0
14	BKD	.0028	04.1	44.1	7.38	21.7	.733	.151	.222	04.5	67.0	4.00	11.0	20.0	38.0
15	BJJ	.0035	04.4	61.1	7.11	21.3	.739	.151	.216	04.5	66.0	4.10	10.5	19.5	38.0
22	BJG	.0032	04.2	61.4	7.15	22.1	.741	.154	.227	04.6	56.0	3.93	11.0	20.0	38.0
23	CCD	.0026	03.7	61.0	7.45	22.1	.741	.153	.228	04.5	58.0	3.96	11.5	19.5	38.0
24	CEF	.0044	05.0	49.1	7.43	21.4	.734	.151	.218	04.5	68.0	4.14	11.0	19.2	36.0
26	BGA	.0062	04.4	61.4	7.37	21.1	.733	.146	.208	04.5	76.0	4.08	12.0	19.0	38.0

TABLE II

2N1708 ELECTRICAL SPECIFICATIONS

T_J	V_{CBO}	V_{CEO}	V_{EBO}	I_C	P_d (T_A=25°C)
-65°C to 175°C	25v (max)	12v (max)	3v (max.)	200ma (max.)	3 watts (max.)

Characteristics T_A = 25°C +	Conditions	Limits		Units
		Min.	Max.	
I_{CBO}	V_{CB}=15v, I_E = 0		0.025	μa
I_{CBO}	V_{CB}=15v, I_E = 0, T_A = 150°C		15.0	μa
I_{CEX}	V_{CE}=10v, V_{BE} = -.25v, T_A = 100°C		15.0	μa
BV_{CBO}	I_C = 100μa	25.0		v
BV_{EBO}	I_E = 100μa	3.0		v
BV_{CEO}	I_C = 10ma	12.0		v
V_{BE}(Sat.)	I_C = 10ma, I_B = 1ma	0.7	0.9	v
V_{CE}(Sat.)	I_C = 10ma, I_B = 1ma		0.22	v
V_{CE}(Sat.)	I_C = 50ma, I_B = 5ma		0.35	v
C_{ob}	V_{CB} = 10v, I_B = 0, f = 140kc		6.0	pf
h_{FE}	I_C = 10ma, V_{CE} = 1v	20.0		
h_{fe}	I_C = 10ma, V_{CE} = 10v, f = 100mc	2.0		
t_s	I_C = I_{B1} = I_{B2} = 10ma R_C = 1000Ω, V_{CE} = 10v		25.0	n sec.
t_{on}	I_C = 10ma, I_{B1} = 3ma, I_{B2} = 1ma V_{CC} = 3v, R_C = 270Ω		40.0	n sec.
t_{off}	I_C = 10ma, I_{B1} = 3ma, I_{B2} = 1ma V_{CC} = 3v, R_C = 270Ω		75.0	n sec.

+Unless otherwise specified

III. DEVICE PROCESSING

A. Photoresist and Etching Techniques (A. Warren)

As a result of investigations to determine the most suitable method of removing photoresist without leaving contaminants on the wafer or damaging the wafer surface, the following procedure has been standardized and is presently being used:

1. The major portion of photoresist material is removed by gently scrubbing the wafer with methylene chloride.
2. To remove the small residues left from the scrubbing operation, the wafer is sprayed with triple distilled chloroform and heated air. The heated air is used to dry the wafer, preventing frost formation. Any further residues remaining are then burned off leaving the wafer surface as free of contamination as possible.

An evaluation of an alternate photoresist technique to obtain aluminum contacts was performed. The technique involved evaporating aluminum over the wafer and then removing the aluminum with Na OH in the undesirable areas. By this procedure it was anticipated that an improvement in reliability might be achieved through a reduction in contamination believed associated with the existing process. Also, it was possible to obtain thicker aluminum contacts as discussed in Section III C and D. An additional photoresist step was required that was not necessary in the existing process. It was found that the disadvantages of the additional photoresist step outweighed the advantages. The additional step resulted in decreased yields. Also, it became apparent that evaporating

aluminum directly on the oxide increased the possibility of the aluminum entering any pinholes which may inadvertantly exist in the oxide. In addition, the photoresist removal method described previously has reduced the possibility of contamination.

The above investigation completes the process improvements in the area. The photoresist process, as presently standardized, will satisfactorily meet the reliability goals of the contract.

The process improvements initiated in this area are:

1. The improved technique of photoresist removal as described above.
2. Chemicals used in the photoresist operation are filtered to remove impurities just prior to being used.
3. More critical inspection of the photoresist masks to insure proper definition and less pinholes. This operation also includes a visual inspection of the mask just before it is used to detect any dust or other foreign matter on the mask or wafer that would be harmful to the exposure pattern or wafer surface.
4. Close control of the whirler rotational speed utilizing a tachometer. The whirler speed is closely controlled during KRP applications to maintain consistent photoresist thickness.
5. A double coating of KPR is applied which greatly reduces the number of pin holes in the photoresist which would, when

exposed, cause pin holes in the protective oxide layer.

6. Control of the intensity of the exposure light. The intensity of the exposure light is checked periodically to ensure that the proper amount of light and the proper wave length of light are being used to expose the photoresist patterns.

B. Surface Preparation and Cleaning (W. Kern)

A summary is presented of selected experimental results obtained from radiochemical surface studies conducted by the Advanced Development Laboratory of RCA, Somerville. This completes the surface preparation and cleaning studies performed in connection with the program. Many process improvements have been effected as a result of the work as noted in previous Quarterly Reports and as summarized at the end of this section.

1. Inorganic Reagent Materials as Sources of Semiconductor Surface Contamination

It is well known that fractional monoionic layers of impurities on a semiconductor surface can have pronounced effects on the electrical device properties. Obviously, conventional methods of analysis cannot be used for quantitative investigations at these extremely low concentration levels. Radiochemical methods, on the other hand, are sensitive, specific, and simple. They have been used to great advantage to study adsorption and desorption processes.

The results were used for the development of methods for removing contaminants from solutions and device surfaces.

Materials and devices were processed by standard methods, but the various reagents were labeled by the addition of radioactive isotopes. After treatment, the adhering reagent was rinsed off under standarized conditions, and the radioactivity on the samples was measured with a suitable nuclear counting instrument. From the counting rate and the previously determined specific activity of the reagent, (radioactivity per unit weight of substance traced), the average surface impurity concentration was computed. The distribution of a radioactive impurity on the sample surfaces was determined by microprobe counting and by autoradiographic techniques. For the latter, the samples were placed on a photographic emulsion sensitive to the emitted radiation; development of the photographic film produced images of the distribution of the radioactive material. After these initial examinations, the samples were subjected to various kinds of rinsing treatments to determine the rates of desorption of the active impurity with water, acids, organic solvents, and complexing or chelating agents at various temperatures. Mechanical rinsing parameters included simple stirring, cascade treatments, counter-current-flow systems, and ultrasonic agitation. In all cases the radio-activity on the sample served as an accurate measure of the residual impurity surface concentration.

In these studies both the main constituents of standard etch solutions and the trace impurities contained in them were

labeled isotopically. For the tracing of ions or molecules of main constituents, sodium-22 or -24 was used in the case of sodium hydroxide; flurcine-18 for hydrofluoric acid-containing etches; chlorine-38 for hydrochloric acid; iodine-131 for etch solutions with iodine; and carbon-14 tagged acetic acid for etches containing this acid. Fluorine-18, a positron emitter with a half-life of only 112 minutes, was prepared at Brookhaven National Laboratories by neutron bombardment of $Li_2^6CO_3$; the high-energy tritium nuclei resulting from the $Li^6(n,\alpha)H3$ reaction caused a nuclear transformation of the oxygen to fluorine-18: $O^{16}(t,n)F^{18}$. Radioactive hydrofluoric acid was prepared and purified by ion-exhange chromatrography and then used in the etch mixture. Chlorine-38, a radioactive isotope of chlorine with a half-life of only 36 minutes, was made by thermal neutron bombardment of sodium chloride, followed by ion exchange to hydrochloric acid; all work was performed directly at the RCA reactor facilities at the Industrial Reactor Laboratories because of the short half-life of this nuclide; gamma spectrometry was used exclusively for radiation analysis. Iodine-131 with a half-life of 8 days posed no special problems.

Adsorption analyses of trace impurities were relatively simple in comparison to those of the main constituents because much higher specific activities could be used and greater sensitivity resulted. A selection of results for important metallic

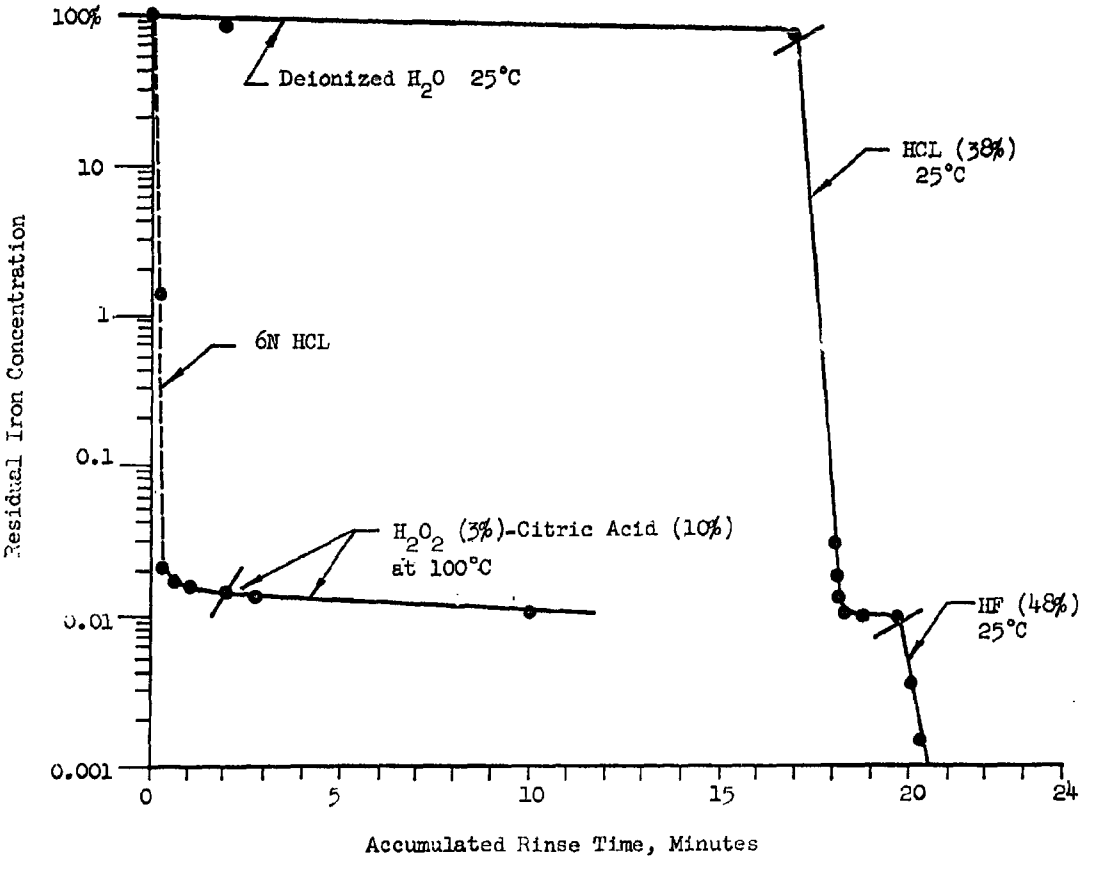
ions on silicon and germanium is presented in condensed form in Table III. Typical desorption curves for the removal of these contaminants by various rinsing agents are presented in Figures 1 and 2. Conclusions concerning the observed concentrations of impurities on silicon surfaces are as follows:

a. Gold

Silicon wafers immersed in concentrated aqua regia, HCl, HNO_3, 30% H_2O_2, 5% NaOH, HF-HNO_3 mixtures, and CP4-type etch mixtures containing 3 to 8 ppm Au labeled with Au^{198} were contaminated to the extent of 10^{12} to 10^{15} Au atoms/cm^2. These concentrations correspond to approximately 0.01 to 10 monoatomic layers. Elemented gold deposited was from HF, NaOH, and H_2O_2 solution. Desorption was most effectively accomplished with HCl-H_2O_2 mixtures or cyanide-containing solutions.

b. Chromium

Silicon wafers immersed at 95°C in H_2O_2 (30%) containing 2ppm of Cr added as $Cr^{51}Cl_3$ had average surface concentrations in the low 10^{15} Cr atoms/cm^2. Autoradiographic analysis showed that these deposits were distributed in the form of strongly localized dots that were difficult to remove by chemical rinsing treatments. Silicon wafers exposed to an HF solution containing 2ppm of Cr attained concentrations in the order of 10^{14} Cr atoms/cm^2. Wafers etched in HF-HNO_3 mixtures of CP4-type solutions containing 2ppm of Cr were



Lapped p-type Si etched 1 minute at 100°C in 5% NaOH (3.7 ppm Fe)
100% = 6.4×10^{15} Fe (atoms/cm^2)

FIGURE 1 DESORPTION OF IRON FROM SILICON WAFERS

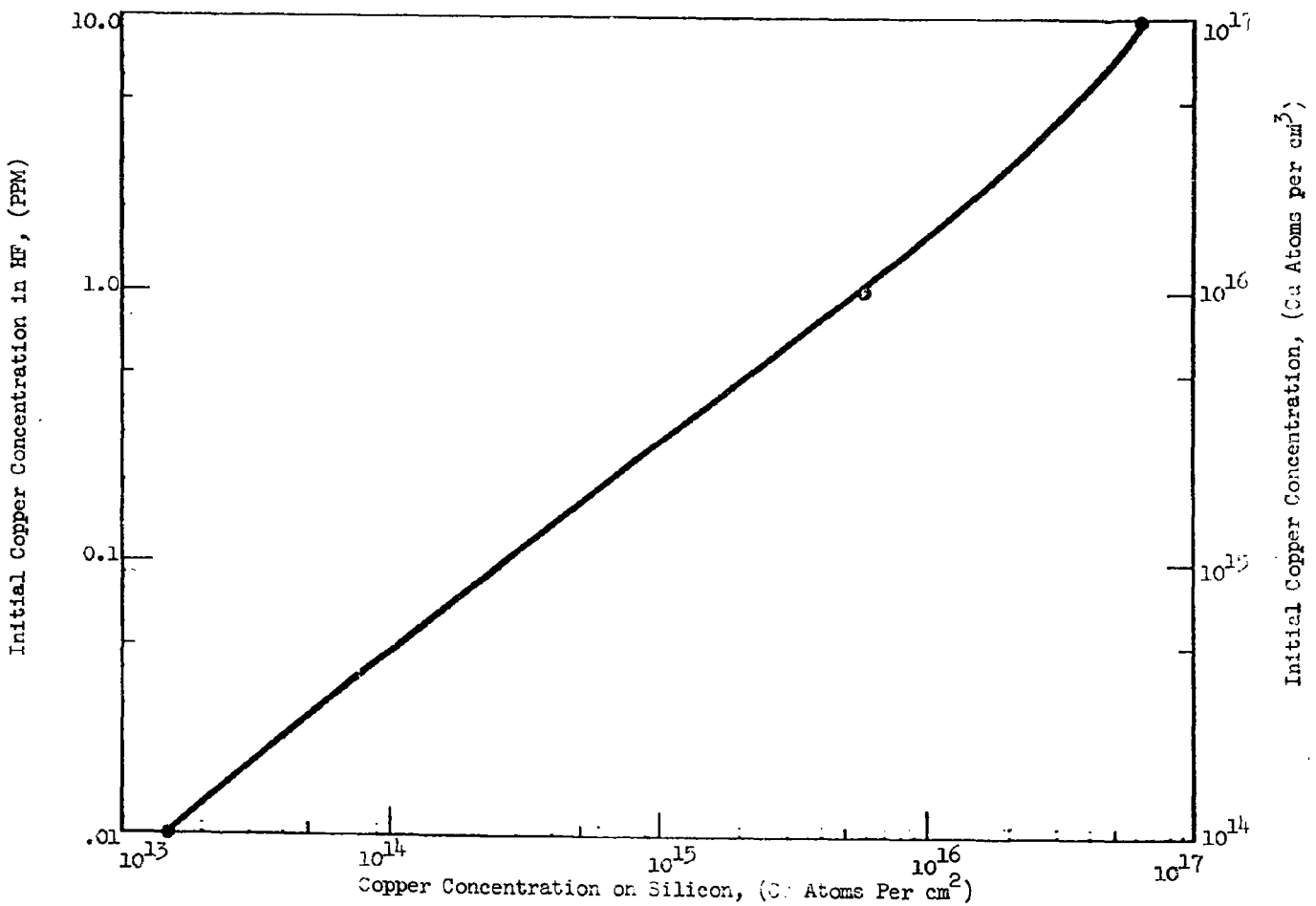


FIGURE 2 DEPOSITION OF COPPER ON SILICON AS A FUNCTION OF SOLUTION CONCENTRATION

contaminated to the extent of 10^{12} to 10^{13} Cr atoms/cm^2; these layers were strongly chemisorbed. Silicon boiled in Chromerge-H_2SO_4 and exhaustively rinsed with deionized water had less than 10^{14} Cr atoms/cm^2, (probably less than 10^{13}).

c. Iron

Silicon wafers (p-type, 6-8 ohm-cm) etched in HF, HCl, HF-HNO_3-CH_3CO_2H mixtures containing 4ppm of Fe added as $Fe^{59}Cl_3$ showed surface concentrations in the order of 10^{10} to 10^{11} Fe atoms/cm^2. Wafers etched for 60 seconds in 5% NaOH at 100°C showed contamination levels of 10^{14} Fe atoms/cm^2; the surface concentration was found to be directly proportional to the Fe solution concentration within the range of 0.01 to 4ppm of Fe in 0.05 to 5% NaOH. Desorption rates with deionized water at 23°C had a half-time of 68 minutes. HCl was much more effective, diminishing the adsorbates in 15 seconds to values of 0.01 to 1% of the original. Final concentrations were usually in the range of 10^{11} Fe atoms/cm^2. Typical desorption curves are shown in Figure 1.

d. Sodium

Etching of various types of silicon wafers in 5% NaOH at 1100°C for 60 seconds led to an average surface concentration of 2×10^{14} Na ions/cm^2. A 15-second rinse in 6NHCl reduced this concentration to 6%; additional rinsing with acid or water reduces this level within

a few minutes to below 0.7%, or $< 8 \times 10^{11}$ Na^+ atoms/cm, which is less than 0.001 of one monoionic layer. Immersion of wafers in 5% NaOH(23°C) solutions led to an equilibrium surface concentration of 8×10^{13} Na ions/cm^2, following a typical Freundlich-type adsorption isotherm.

e. Copper

Contamination by copper was studied with Cu^{64} for many of the common silicon etchants and found to be severe in most instances, frequently reversible only by treatments with chelating solutions, of which the following were found particularly effective from a list of 15 compounds: potassium cyanide, disodium ethylene diamine tetraacetate, citric acid, hydrogen peroxide-formic acid, and N, N-di ($C\beta$-hydroxy-ethyl) glycine sodium salt.

The relationship between Cu surface concentration on silicon and the Cu ion solution concentration in HF is graphically presented in Figure 2.

f. Manganese

Silicon wafers etched for 100 seconds in standard CP4-type solut'ons containing 0.1 ppm of Mn added as $Mn^{54}Cl_2$ showed surface concentrations of below 10^8Mn ions/cm^2.

g. Antimony

Silicon wafers etched in hot 5% NaOH, containing 3 ppm of Sb showed surface concentrations in the order of 10^{13}

Sb atoms/cm^2. The adsorbates were readily desorbed (95% in 30 seconds) with 6 N HCl.

h. Fluorine

Dilute HF and HF-containing etches were labeled with HF^{18} and used for treating silicon wafers. The wafers were given a 30-second rinsing sequence in distilled water before the radiocounting. Immersion of wafers in 1N HF led to surface concentrations of 10^{16} F ions/cm^2, readily desorbable with cold or hot distilled water. Etching for 60 seconds in $HF-HNO_3-CH_3CO_2H$ mixtures or CP4-type solutions led to 10^{14} F atoms /cm^2 of strongly adsorbed layers; rinsing in distilled water at 23°C for 15 minutes removed only 47%.

On the basis of these investigations, practical methods have been developed at RCA and are being employed in the reliability improvement program to eliminate or reduce surface contamination. These procedures are based on the following three main approaches: (1) ultra-purification of chemical etch components by ion-exchange, chromatrography, and distillation in quartz; (2) use of inert and specially cleaned reaction vessels and handling tools; and (3) application of highly developed chemical desorption and rinsing treatments.

TABLE III

CONTAMINATION OF SEMICONDUCTOR SURFACES BY SELECTED METAL IONS DURING CHEMICAL SURFACE TREATMENTS

Semiconductors	Reagent	Radiotracer	Conditions[+]	Impurity Atoms[++]
Silicon Wafers, p-type 2 to 9 ohm-cm resistivity	HF 49%	4.5ppm Fe^{59}	30 min. 23°C	1.3×10^{11} Fe/cm^2
	HF 49%	6.2ppm Au^{198}	30 min. 23°C	2.2×10^{15} Au/cm^2
	HF 49%	2.3ppm Cr^{51}	30 min. 23°C	2.2×10^{14} Cr/cm^2
	HCl 19%	3.7ppm Fe^{59}	30 min. 23°C	2.8×10^{11} Fe/cm^2
	HCl 37%	3.1ppm Au^{198}	15 min. 23°C	2.4×10^{12} Au/cm^2
	HNO_3 70%	3.1ppm Au^{198}	15 min. 23°C	1.9×10^{12} Au/cm^2
	NaOH 5%	3.7ppm Fe^{59}	60 sec. 100°C	6.4×10^{15} Fe/cm^2
		10ppm Au^{198}	60 sec. 100°C	3.3×10^{15} Au/cm^2
	H_2O_2 3%	2.3ppm Cr^{51}	15 min. 95°C	1.6×10^{15} Cr/cm^2
	93 vol. HNO_3 70% + 7 vol. HF 49%	6.2ppm Au^{198}	15 min. 23°C	7.4×10^{13} Au/cm^2
		2.3ppm Cr^{51}	100 sec. 23°C	4.5×10^{12} Cr/cm^2
	Iodine Etch[+++]	6.2ppm Au^{198}	60 sec. 23°C	2.0×10^{14} Au/cm^2
		2.3ppm Cr^{51}	60 sec. 23°C	3.9×10^{12} Cr/cm^2
Germanium Wafers p-type, 1 to 5 ohm-cm resistivity	HF 49%	2.3ppm Cr^{51}	30 min. 23°C	1.6×10^{14} Cr/cm^2
	HCl 18%	3.7ppm Fe^{59}	30 min. 23°C	5.6×10^{10} Fe/cm^2
	NaOH 5%	1.0ppm Fe^{59}	60 sec. 100°C	8.6×10^{13} Fe/cm^2
	93 vol. HNO_3 70% + 5 vol. HF 49%	6.2ppm Au^{198}	15 min. 23°C	1.7×10^{14} Au/cm^2
	95 vol. HNO_3 70% + 5 vol. HF 49%	2.3ppm Cr^{51}	100 sec. 23°C	2.4×10^{13} Cr/cm^2
	Iodine Etch[+++]	6.2ppm Au^{198}	60 sec. 23°C	2.8×10^{13} Au/cm^2
		2.3ppm Cr^{51}	60 sec. 23°C	4.5×10^{12} Cr/cm^2

\+ 0.5 to 5 ml solution per cm^2 sample area.

++ Number of atoms per cm^2 geometric surface area after 1/2 min. of water rinsing.

+++ Mixture of 100 ml HF 49%, 100 ml HNO_3 70%, 140 ml CH_3COOH, 0.5 gm iodine crystals, 0.8 ml Triton -X100 Nonionic Wetting Agent.

C. Contact Preparation (G. Granger)

Three approaches were undertaken to eliminate or inhibit the formation of the intermetallic compound ("purple plague") which forms between connector lead and contact metallization. These were:

1. Thin aluminum contacts - to reduce the ratio of aluminum to gold and thereby inhibit the formation of the "purple plague".
2. Gold contacts - to eliminate the bimetallic system of aluminum contacts and gold wire which forms "purple plague".
3. Thick aluminum contacts - to permit the use of a gold alloy wire which was believed to inhibit the formation of the "purple plague".

Investigation in the contact areas is now considered complete. Further discussion on these three approaches is given below.

1. Thin Aluminum Contacts

The use of thin aluminum contacts was the most successful of the three approaches. Units made with thin aluminum contacts bonded with gold wire and encapsulated have been evaluated on 300°C shelf life for similar unit for 8000 hours. There have been no failures in 67 units tested to end points of $I_{CBO} > 500$ nA and $I_B \geq .667$ (See Section VC Table VIII HK test). This process will be used for making the device which will be evaluated in the production phase of the program.

2. Gold Contacts

When gold contacts were subjected to high temperature life tests, the devices failed because of an open and intermittent problem which was accompanied by severe discoloration of the contact. The discoloration could be inhibited by the addition of small quantities of palladium to the gold which is to be evaporated.

This did not eliminate the problem, however, and all work with gold contacts was curtailed except the completion of evaluation of the life tests.

The results of life test evaluation which were partially presented in the Third Quarterly Report are shown below as completed.

First Designed Experiment

Cell No.	Type of Test	Sample Size	Down Period			
			100 Hrs.	250 Hrs.	500 Hrs.	1000 Hrs.
1	300°C	25	0	3	1	0
	300 mw	25	0	0	0	0
2	300°C	25	0	0	0	1
	300 mw	25	0	0	0	0
3	300°C	25	9	2	2	6
	300 mw	25	2	2	6	3
4	300°C	25	3	0	1	1
	300 mw	25	0	0	0	2

Second Designed Experiment

Cell No.	Type of Test	Sample Size	Down Period - 500 Hrs.
2	300°C	31	3
3	300°C	37	16

After 500 hours, the test was discontinued. The majority of units (>90%) which failed in Cell No. 3 on both designed experiments and Cell No. 4 on the first designed experiment were open or intermittent units. The others exhibit the same failure modes as units with aluminum contacts.

3. Thick Aluminum Contacts

Units were made with aluminum contacts which were 40,000 Å thick in order to evaluate a gold alloy wire which could be successfully bonded to a thicker contact only. An evaluation is given in the next section on this part of the investigation. The process concerned with obtaining heavy aluminum contact was not desirable because it was difficult to control (See Section III-A Photoresist).

D. Bonding (G.Granger)

The program which was initiated in the bonding area included the evaluation of:

1. Gold alloy wire - for the reasons stated in the section on contact preparation (Section IIIC).
2. Nailhead bonding of gold wire - to improve the bond strength and increase bonding efficiency.
3. Bonding gold wire to thin aluminum - to inhibit the formation of the "purple plague".

As stated in the section on contact metallization (Section IIIC) the process which was most successful was the last one and this process will be used for making devices in the production phase of this program.

The results obtained on each of the above approaches are as follows:

1. Gold Alloy Wire

A group of devices, which were made with aluminum contacts, were bonded with gold alloy wire and evaluated for bond strength after being subjected to 300°C shelf life. This evaluation was performed by placing the entire test on 300°C shelf life, removing

a random sample from the test at scheduled intervals, and subjecting these units to a bond strength test. Since the bond strength test is destructive, the characteristic bond strength of the entire group is represented by a different sample at each interval.

A graph of the average bond strength at each evaluation interval is shown in Figure 3. As indicated, the bond strength decreases with time on high temperature shelf life to a point where it is less than one-quarter of the original bond strength at 200 hours. Similar results were obtained with devices which were made with pure gold wire and thin aluminum contacts. Data obtained on these units are shown on the graph of Figure 3 for zero hours and 64 hours on 300°C shelf life.

The decrease in bond strength is independent of connector material. It is believed that the gold alloy wire causes visual inhibitation of the discoloration. However, the strength of the bond is not materially improved by the alloy.

Since little would be gained in bond strength by changing the device to gold alloy wire and a possible overall loss in reliability (due to the increased complexity of the metallization process required for this design), this approach was abandoned.

2. Nailhead Bonding

The diameter of the connector wire must be decreased to reduce the diameter of the nailhead enough to fit the metallization pattern. Gold wire, with reduced diameter, was obtained and a sample was bonded using the nailhead bonding process. The sample indicated that bonding to this device would be feasible. When

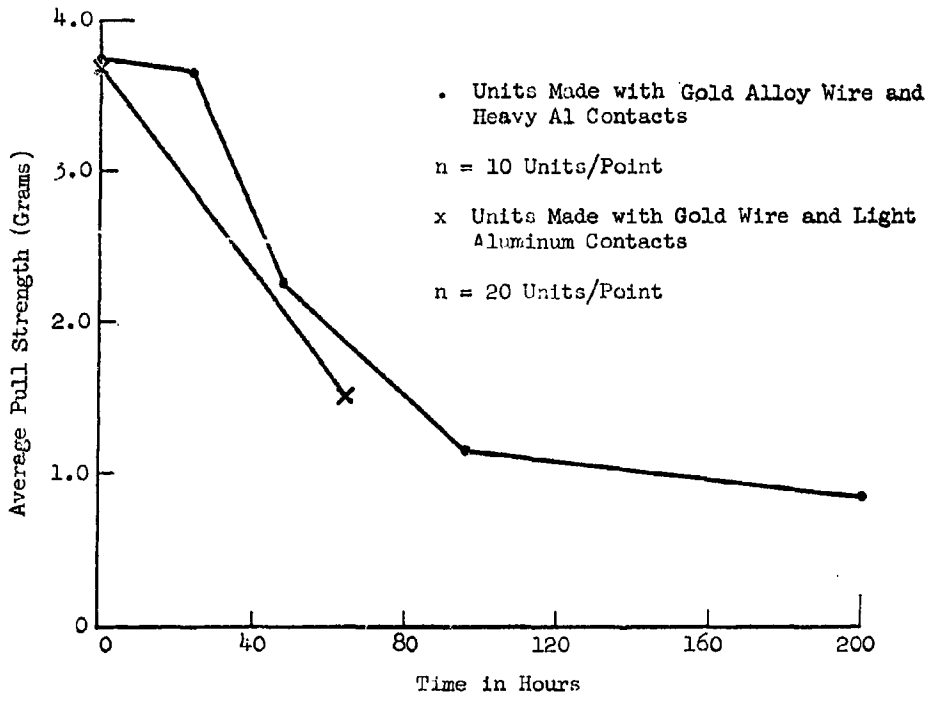


FIGURE 3 AVERAGE BOND STRENGTH vs. TIME ON 300°C SHELF LIFE-2N1708

larger lots were processed for production purposes, it was determined that the reduction in size was not sufficient. Although the nailhead was small enough to fit the pattern and successful bonds could be made, the clearance was insufficient to obtain consistant results.

3. Bonding Gold Wire to Thin Aluminum

A discussion of this process is presented in Section IIIC. Data is given in Section VC, Table VIII.

An additional study was performed to determine the change of bond strength on high temperature shelf life. A group of 30 units from one lot was divided into three parts. These were: (1) tested for bond strength at zero hours; (2) tested for bond strength after 16 hours on 300°C shelf life; and (3) encapsulated and then subjected to the same treatment as the second part of this test. A histogram of the results of bond strength measurements for each group is shown in Figure 4. It can be seen that degradation of bond strength has been improved due to encapsulation.

Failure analysis of units which have been processed with an encapsulant show the devices do not fail because of degradation of the bond. A significant reduction in failure rate on high temperature life tests has been achieved resulting in a bonding technique capable of meeting the reliability goals of the contract.

E. Sealing (G. Granger)

1. Dessicant Evaluation

On initial tests, more failures occurred on the group of devices with a dessicant in the shell than without a dessicant when the

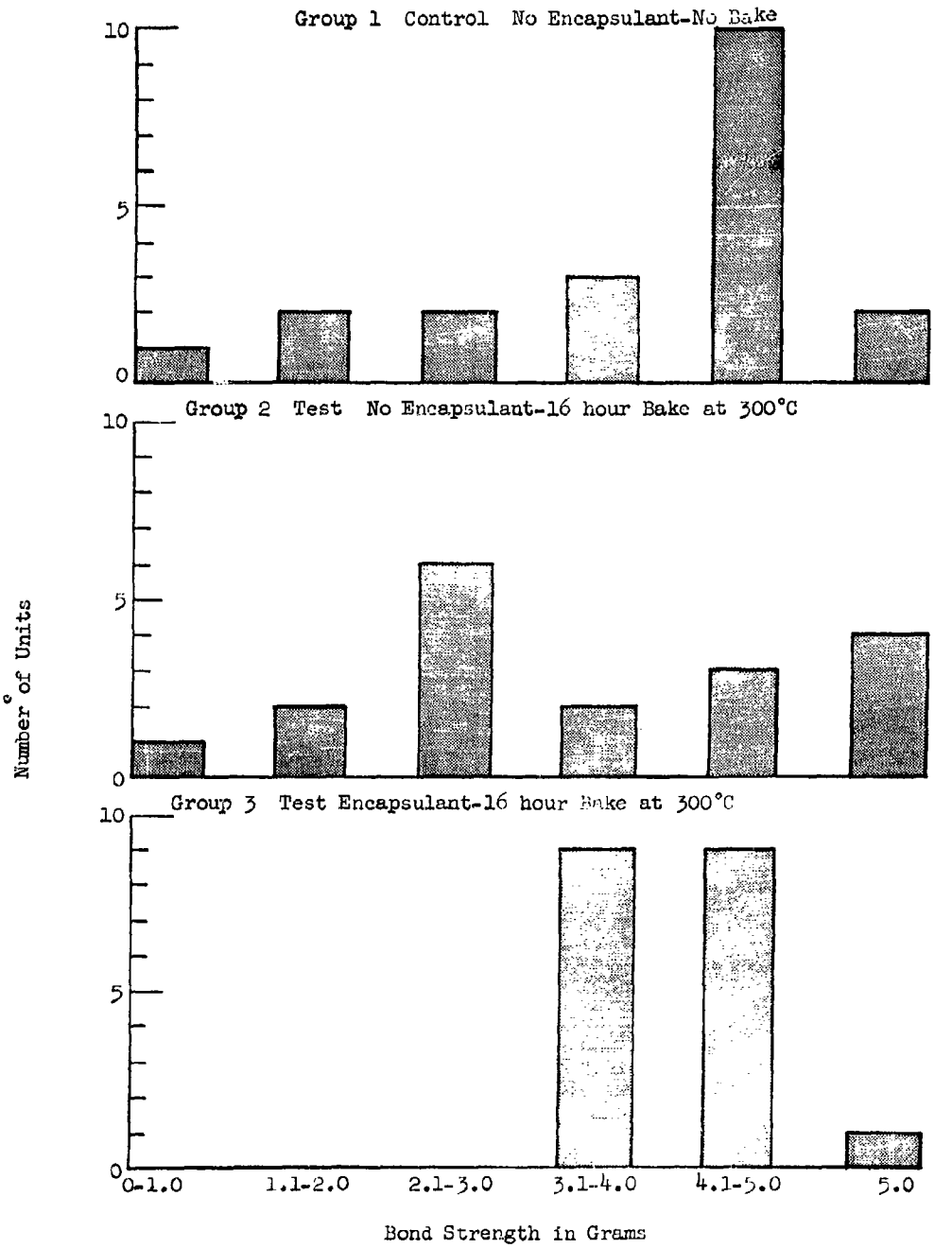


FIGURE 4 HISTOGRAM ON BOND STRENGTH EVALUATION

devices were placed on high temperature shelf life. The test was repeated with a more active dessicant and the same results were obtained. Since all of the dessicants evaluated were of the reversible type, it is believed that moisture was released from the dessicant when the devices were subjected to a high temperature environment after sealing causing the failure rate to increase rather than decrease.

2. Encapsulation Evaluation

The best results on high temperature shelf life are attained when the device is encapsulated. This is shown by the results of Section VA where the devices of lot PF which were encapsulated were superior to the devices of lot AG which were not encapsulated when these were evaluated on high temperature shelf life. In addition, two engineering tests were performed to evaluate encapsulation. Units in these tests were completely randomized to eliminate process variables other than the encapsulation bake process. The devices encapsulated were superior to the non-encapsulated units on high temperature shelf life as shown below.

300°C SHELF LIFE ATTRIBUTE DATA
NUMBER OF FAILURES+ AT EACH DOWN PERIOD

Test	Device Description	Sample Size	Down Period - Hours 100	250	500	1000	Test No.
Experiment No.3 I_{CBO} >.500μA Non-Encapsulated or h_{fe}< 15	Encapsulated	25	0	0	0	1	1
	Encapsulated	25	0	3	1	0	
Lot PG I_{CBO} >.010μA Non-Encapsulated or h_{fe}> 15	Encapsulated	20	0	0	1	-	2
	Encapsulated	20	1	1	5	-	

Other data on the second test supporting these conclusions is shown in Section VF- Variables Data.

+ Note: The term failures is used loosely here to describe units which have exceeded the limits shown.

When the devices were evaluated on operating life, it was determined that better results were obtained on the non-encapsulated units. This is shown on operating step stress tests where failures+ occurred on encapsulated devices at lower stresses on lot PF and failures did not occur in the same region on lot AG which was not encapsulated (see Section VG for this comparison). As confirmation of this, an evaluation was made on 300 mw operating life where the following results were obtained.

Lot	Sample Size	No. of Failures +	
		I_{CBO} 10n amps	I_{CBO} 25n amps
AG	60	0	0
PF	60	3	1

In addition, the following failures+ were experienced on 300 mw operating life on units run as part of Experiment No. 3 noted above.

Experiment No. 3	Sample Size	No. of Failures +	
		I_{CBO} 10n amps	I_{CBO} 25n amps
Non-Encapsulated	25	0	0
Encapsulated	25	1	1

In order to effect an improvement in the device on operating life, without a detrimental effect on the high temperature life of the device, an improved encapsulant has been incorporated into the standard process. This change is being made on the basis of results obtained after 250 hours of operating and

+ Note: The term failure is used loosely here to describe units which have exceeded the limits shown.

high temperature shelf life tests on a device similar to the 2N1708. These results show a significant difference in I_{CBO} on the operating life tests at a 90% confidence level, proving the new encapsulant better with no significant difference in I_{CBO} on the high temperature life tests or h_{FE} on either of the life tests. Further, the new encapsulant is the same basic material as the old encapsulant but of a higher purity grade.

All of the investigations in the sealing area are complete. The process will satisfactorily meet the reliability goals of the contract.

F. Ceramic Stem (G.Granger)

An initial evaluation of the ceramic stem indicated superior qualities (Refer to Quarterly Report No.1). When production was increased, however, problems developed. Because of these problems, a design for a suitable glass to metal stem was established. Results to date indicate this stem to be completely satisfactory. This has been shown by failure analysis where no failures have been traced to the stem.

Although engineering effort has continued to produce the ceramic stem, and encouraging results have been obtained, it has been decided that it is not to the best interests of the program to begin to evaluate this stem in terms of the reliability goals of the contract. In addition, the initial cost of the ceramic stem is higher than the glass to metal stem, although its cost will certainly decrease with experience.

For these reasons, it is not planned to change from the present

stem design to the ceramic stem. The reliability objective of the contract will be achieved by the glass to metal stem developed earlier in the program.

IV. INSPECTION AND QUALITY CONTROL (P. Grenier)

A Quality Control and Inspection Plan was submitted to the Signal Corps on 24 April 1963.

V. RELIABILITY TESTING AND ANALYSIS

A. Acceleration Factors and Process Evaluation - High Constant Stress Tests - Temperature (G.Granger)

Units selected from three developmental lots on the 2N1708 program were placed on high temperature shelf life tests in order to (1) establish procedures which would permit rapid evaluation of process changes and (2) determine the magnitude of acceleration factors. High temperatures constant stress shelf life tests were chosen in preference to a step stress test because of the simplicity of the constant stress test and the experience in interpretation.

Step stress testing was avoided for several reasons. These were:

(1) When using the step stress test on devices which have a high activation energy, i.e., a steep acceleration curve, for accurate characterization of the failure distribution on the device, the time per step must be increased to the point where the test is almost equivalent to a constant stress test.

(2) The results on a step stress test are difficult to analyze. Analysis must include consideration of the effect of previous steps to establish the effective level of each step.

(3) The increased complexity of test procedure. Continuous surveillance of the test is required to insure that temperatures are correct, and units are scheduled for the proper test at the proper time.

Step stress testing does serve a useful purpose in providing information for establishment of the constant stress test levels in

a minimum of time.

The high temperature constant stress conditions which were selected for this evaluation were 260°C, 300°C, 320°C and 340°C. In addition, two lots were evaluated at temperatures above 340°C in a special variable temperature oven which was specifically designed for this evaluation. The down periods were varied with each test because failures occurred quite rapidly at the extreme high temperature conditions. All units were read and recorded for I_{CBO} at V_{CB} = 15V and h_{FE} at I_B = 0.5, V_{CE} = 1.0 volts at every down period. The data was reviewed after every down period and a record of the attribute data was maintained on each of the lots. An example of this record is shown in Figure 5.

The information from this record was plotted on Weibull probability paper for each lot at each test condition in order to determine the mean failure time or time to 50% failure for each test condition (see Figure 6). The mean failure time was then plotted on semilog paper versus the reciprocal of the shelf life temperature in degrees Kelvin. The points for mean failure time versus $^1/T$ fell extremely close to a straight line for AG and PF (see Figure 7)indicating the validity of this evaluation procedure. Analysis of the failures occurring on these lots showed the same failure mode

Lot No.	Type of Test	Elect Char.	Limits $I_{CBO} > .500\mu A$ $h_{FE} < 15$								
			Down Period - Hours						Total Fails	Weibull Parameters	
			24	48	96	250	500	1000		β	∝
AG	340°C	I_{CBO}	10/20	5/10	4/5	1/1	-	-	20	.9	20
		h_{FE}	0/20	1/20	5/19	9/14	5/5	-	20	1.2	330
		Total	10/20	5/10	4/5	1/1	-	-	20	.9	20
			24	72	226	476	835				
	320°C	I_{CBO}	0/19	0/19	0/19	10/19	3/9	-	13	.45	13.4
		h_{FE}	0/19	0/19	0/19	0/19	1/19	-	1	-	-
		Total	0/19	0/19	0/19	10/19	3/9	-	13	.45	13.4
			24	48	96	250	500	1000			
	300°C	I_{CBO}	0/20	0/20	0/20	0/20	0/20	2/20	2	-	-
		h_{FE}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		Total	0/20	0/20	0/20	0/20	0/20	2/20	2	-	-
	280°C	I_{CBO}	0/20	0/20	0/20			-	0	-	-
		h_{FE}	0/20	0/20	0/20			-	0	-	-
		Total	0/20	0/20	0/20			-	0	-	-
	260°C	I_{CBO}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		h_{FE}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		Total	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
	200°C	I_{CBO}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		h_{FE}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		Total	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
			24	48	112	272	504	1003			
	300 mw 15V	I_{CBO}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		h_{FE}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		Total	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
			24	48	112	272	504	1003			
	300 mw 12V	I_{CBO}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		h_{FE}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		Total	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
	300 mw 6V	I_{CBO}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		h_{FE}	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-
		Total	0/20	0/20	0/20	0/20	0/20	0/20	0	-	-

FIGURE 5 EXAMPLE OF A SUMMARY OF LIFE TEST DATA

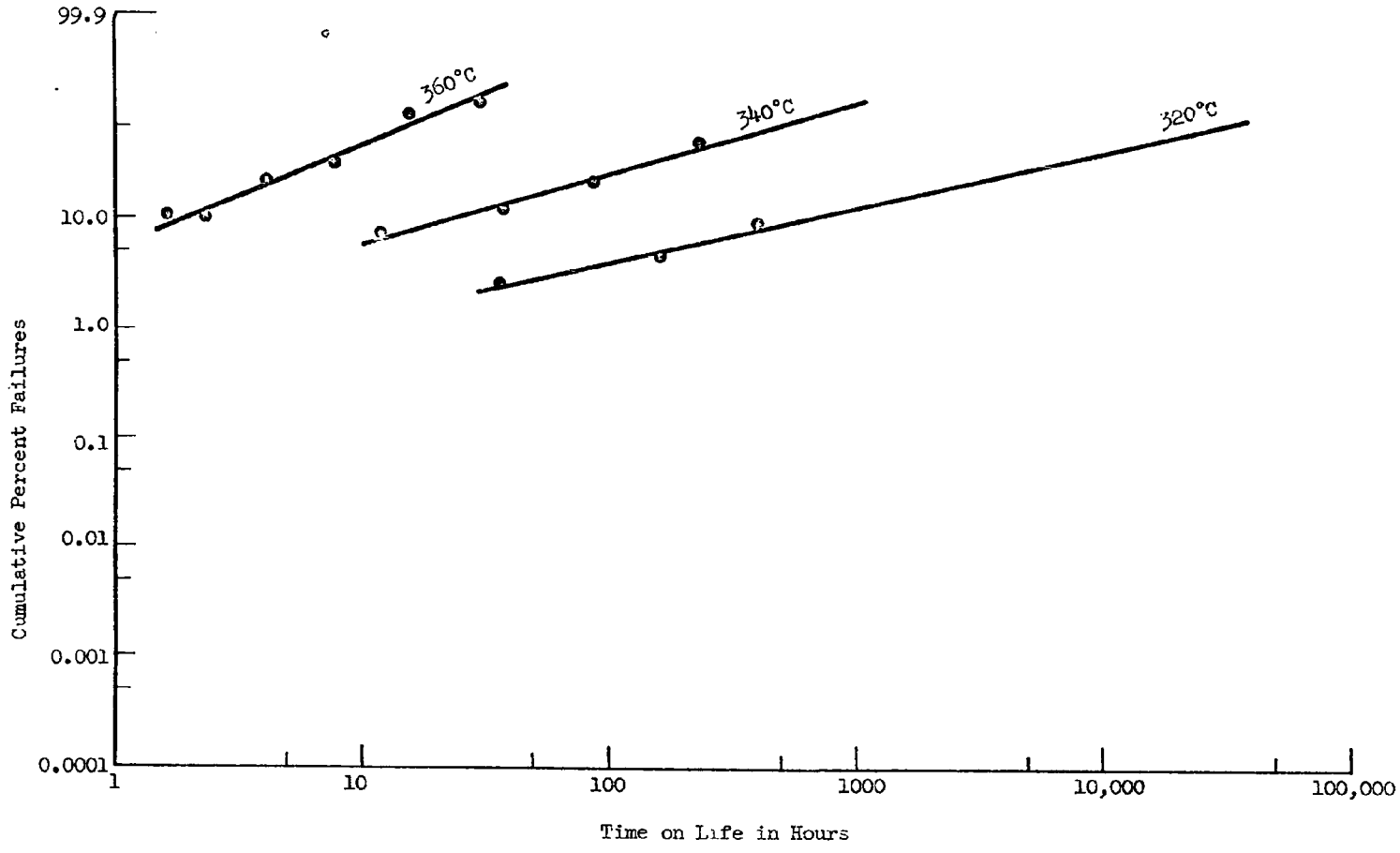


FIGURE 6 GRAPH OF CUMULATIVE FAILURES (Lot PF)

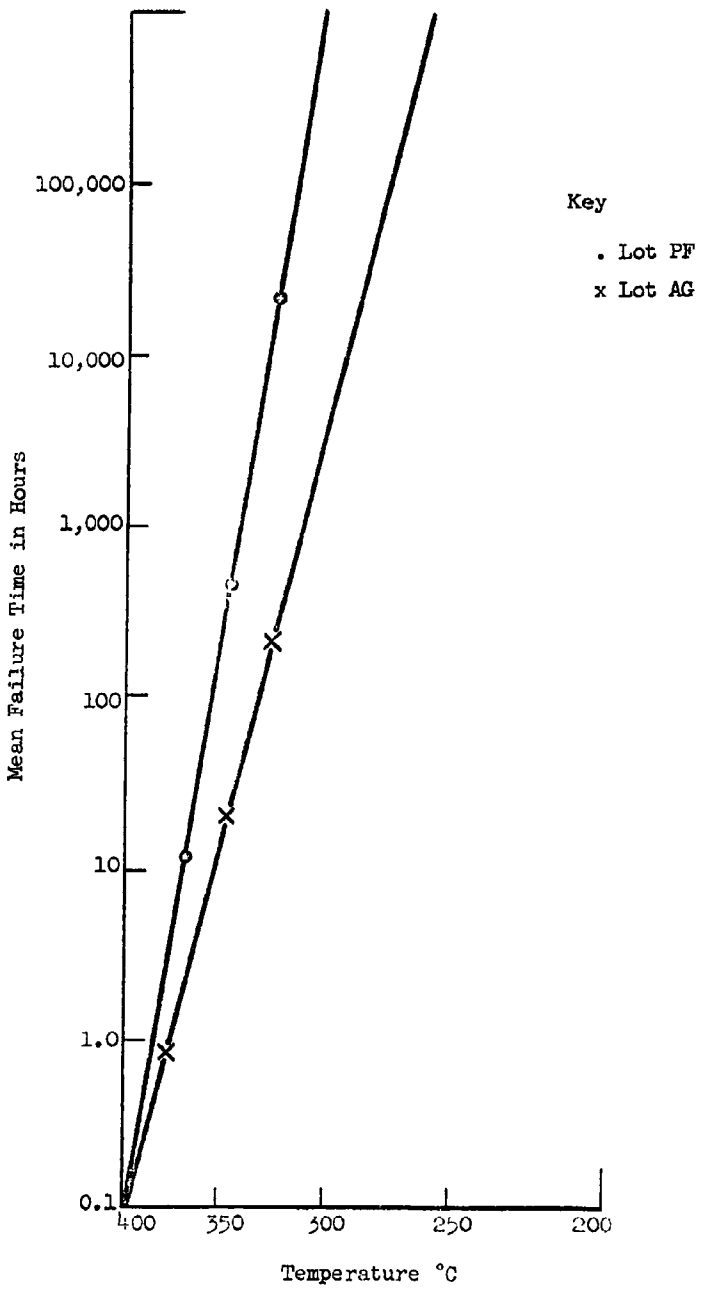


FIGURE 7 GRAPH OF HIGH TEMPERATURE SHELF LIFE - MEAN FAILURE TIME vs. 1/T

to be prevalent at the different levels of high temperature constant stress testing investigated, making connection of the points valid.

The curves of Figure 7 show lot PF to be superior to lot AG. Because of these results and other data on the device, the processing similar to that used on lot PF has been adopted as standard.

The curve of failure rate per 1000 hours vs. $^{1}/_{T}$ can also be obtained from the curves of Figure 6 by determining the cumulative percent failures when each curve crosses the 1000 hour point. This is the average failure rate per 1000 hours for the first 1000 hours on life at each stress. These points are then plotted on Semilog paper vs the reciprocal of the stress in degrees Kelvin as shown in Figure 8 for lot PF. From this curve the acceleration factors for any high temperature life test may be determined. These acceleration factors would then be used in demonstrating reliability of the device at some lower temperature. Extrapolation of the failure rate curve can be made to the 300°C temperature range because it is known that the same failure mode exists in this region. It is believed that extrapolation is valid down to 25°C because no new failure modes have been found in the area between 300°C and 25°C.

It is recognized that the failure rate curve of Figure 8 is extremely steep. However, there is no reason to believe that this is not representative of the device which was investigated because every precaution was taken to insure that each sample was representative of the entire lot. Effort will be devoted to continuation of this investigation for future verification

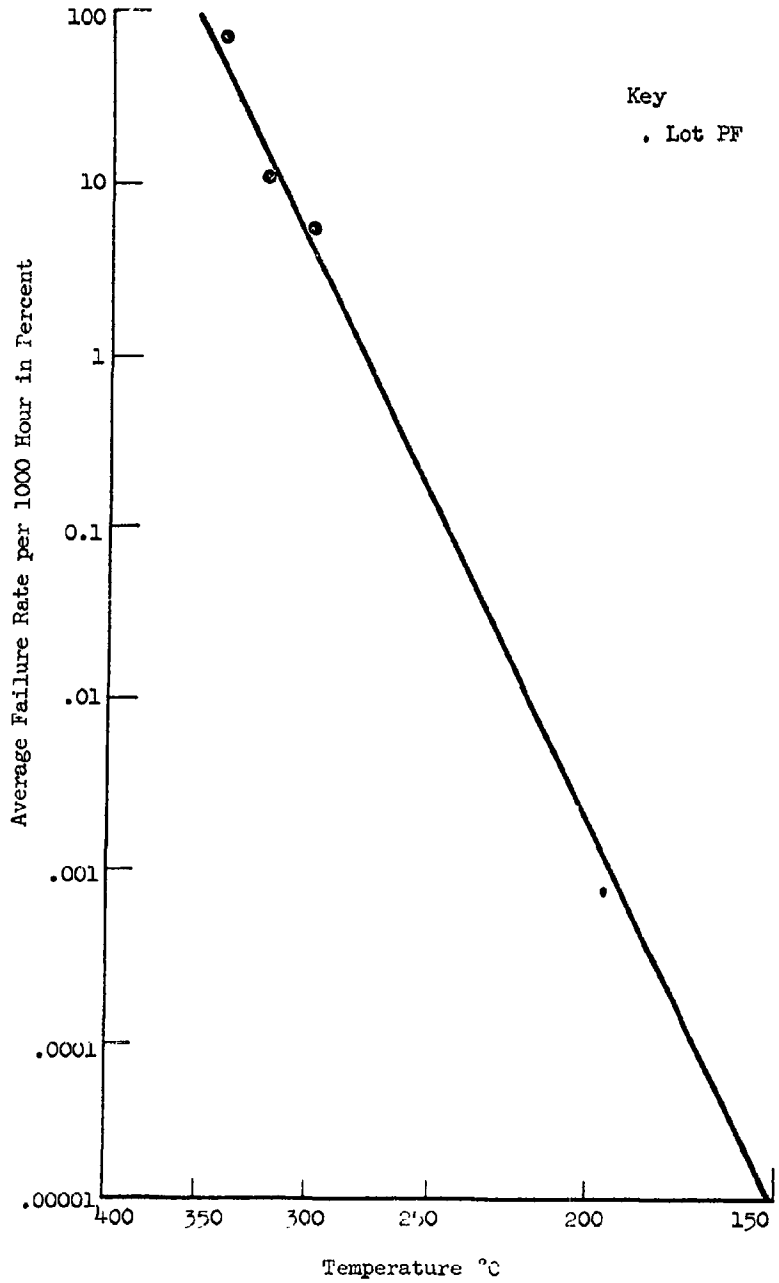


FIGURE 8 GRAPH OF HIGH TEMPERATURE SHELF LIFE - AVERAGE FAILURE RATE vs 1/T

of this data on other lots of similar fabrication.

The development of an acceleration curve for all lots may not be possible if the failure modes are not completely stress dependent. One lot of units which was run on temperature acceleration tests did not show a temperature dependent failure mode in the range of temperatures which were investigated.

These devices were made with gold contacts as mentioned in the section of this report on metallization and it was known that the process was inferior when the devices were placed on high temperature shelf life. The evaluation was conducted to determine the characteristics of the acceleration curve on devices made with an inferior process.

The failure rate per 1000 hours was obtained on random samples of this lot which were subjected to four different high temperature constant stress tests and one low temperature test (25°C). When the high temperature failure rate data was analyzed by the method of least squares, it was shown that the slope of a line through the four points was not significantly different from zero, (see Figure 9). The data obtained on the units which were held at 25°C showed no failures and no shift in electrical characteristics.

It is concluded that the failure mode has changed significantly between 25°C and 260°C making extrapolation of the high temperature data invalid. The activation energy of the high temperature failure mode appears to be quite low.

B. Thermal Resistance Measurements and Variations of Junction Temperature on Life Test (B. Walmsley)

The first part of this section will discuss methods of measurement of thermal resistance and will show which is most applicable to high stress levels of operation; the second part will discuss methods of controlling junction temperature on life so that it is no longer a function of time or position on the life test rack.

1. Methods of Measurement of Thermal Resistance

Method	Temperature Dependence Parameter
A	V_{EB} at I_E = 1mA with collector open circuit
B	I_B at the operating condition
C	V_{EB} at the operating condition
D	V_{BE} at I_E = 1mA - rapid reading method

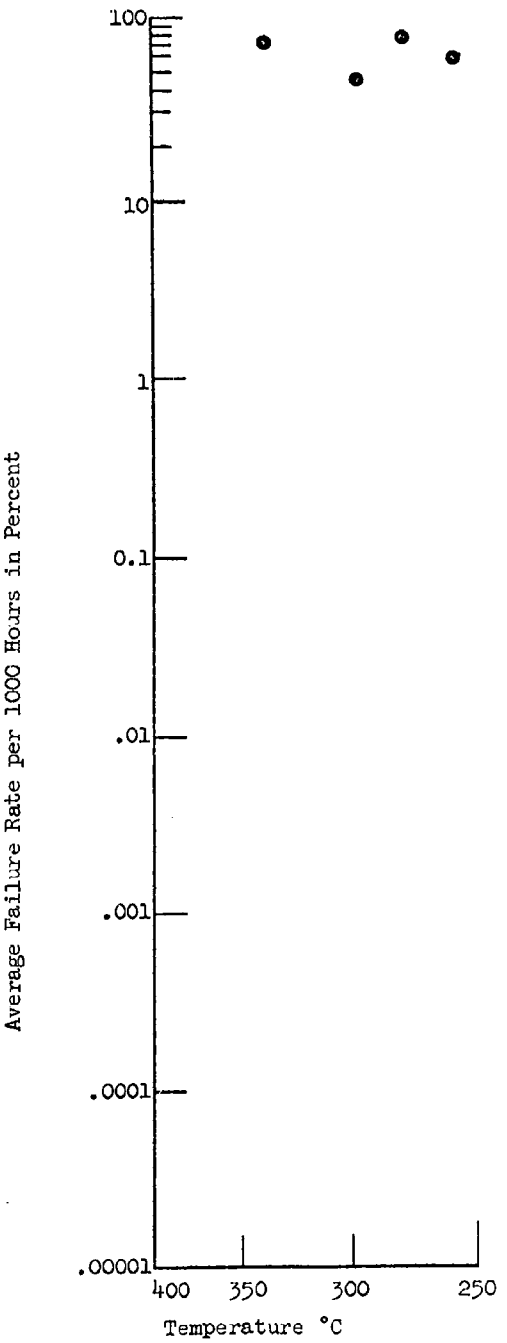


FIGURE 9 HIGH TEMPERATURE SHELF LIFE - AVERAGE FAILURE RATE (IN PERCENT) vs. 1/T

a. Method A - In this method the transistor is switched from a dissipating condition to a measuring condition. It is an essential feature of this method, especially on high frequency transistors, that the junction temperature be sampled within a very short time of switching off the power. This time has been reduced to less than 30μsecs. Readings are repeatable within a few percent providing the ambient is under control and the method can be used for any operating condition (even the abnormal ones which can occur at high stress levels.)

Variation of V_{EB} with temperature is predictable. For the 2N1708, it has been found to be 2mv per °C up to temperatures as high as 300°C.

b. Methods B and C - These methods are very similar in use. In both cases the constant junction temperature or the constant reference temperature methods may be used. The former method is more frequently used, since a calibration is required in the latter. These methods are hampered by certain limitations:

1. In the case of the 2N1708 we are chiefly interested in junction to air thermal resistance, since the transistors are operated in air. Two accurately controlled air ambients are necessary and these are difficult to find without using forced air. Forced air cannot be used since thermal resistance varies very greatly with the velocity of the air moving across the device.

Even in a natural convection ambient, junction-to-air thermal resistance varies with dissipation and this can cause large errors when the constant junction temperature method is used since this method assumes invariance of thermal resistance between the two dissipations.

2. Both methods rely on the temperature dependent parameter being independent of collector voltage. V_{EB} usually is under normal operating conditions, but tests on the 2N1708 showed h_{FE} to increase with voltage.

3. At very high junction temperatures, the increase in h_{FE} and I_{CO}, with temperature, cause I_B to reverse and eventually V_{EB} reverses. Under these abnormal operating conditions, it is likely to be very difficult to apply these methods.

c. Method D (Rapid Reading Method) - This method uses V_{BE} as a temperature dependent parameter, but the measurement is made with a single pulse of power. The transistor is switching from the dissipation condition to a measuring condition, and the first sample of V_{BE} is taken 200μsec after switching. Junction-to-case thermal resistance is measured under normal operating conditions and the method has the advantage of speed.

d. Comparison of Methods - Method A is the most versatile since it can be used for all types of measurement under any conditions. It also measures at a single dissipation

level in a single ambient temperature so that no complications arise due to changes of thermal resistance while measuring. This is the method which has been used for most measurements, although the other methods have been used for comparison of junction-to-case thermal resistances.

Table IV shows the comparison of Methods A and D.

TABLE IV

COMPARISON OF METHODS A AND D

	Thermal Resistance Junction to Case				Junction to Air
	Sampling Time				
	Method A			Method D	Method A
Unit No.	20μsecs. °C/W	50μsecs. °C/W	100μsecs. °C/W	200μsecs. °C/W	20μsecs. °C/W
1	116	105	100	97	450
2	107	95	92	85	500
3	113	101	98	90	473
4	98	87	84	78	428
5	104	94	91	90	453
6	108	95	91	83	450
7	117	107	103	97	460
8	99	87	83	75	430
9	107	95	91	87	425
10	114	101	97	94	460
Average	108	97	93	88	452

The importance of measuring V_{EB} as soon as possible after switching off the power is seen. Method D gives readings which are about 20% lower on the

average.

In comparing Method A with Methods B and C, only junction to case thermal resistances were compared in this investigation since, for reasons mentioned, junction to air thermal resistances by methods B and C are difficult.

Two series of measurements were made: the first with the test transistor immersed directly in an agitated oil bath; and the second with the device clamped to a copper heat sink which was then immersed in the same oil bath. Table V shows results of initial measurements without a heat sink on Unit 7 and Table VI with a heat sink on the same unit. Similar results have been obtained on other units.

TABLE V

RESULTS OF MEASUREMENTS WITHOUT HEAT SINK

Temp. °C	Conditions					Thermal Resistance (°C/W)		
	Vcb volts	Veb volts	Ic mA	Ib μA	Power mw	A	B	C
70	3.01	.709	50	675	186	186		
50	6.26	.721	50	675	349	175	245	
30	6.99	.709	50.5	650	389			197
70	3.03	.720	60	850	225	176		
50	5.58	.731	60	850	378	171	261	
30	6.16	.720	60	810	413			212
70	3.02	.728	70	1000	262	178		
50	5.28	.737	70	1000	421	171	252	
30	5.71	.728	68	980	438			227
70	3.02	.731	80	1150	300	177		
50	5.24	.738	80	1150	478	158	225	
30	5.53	.731	81	1120	507			193

TABLE VI

RESULT OF MEASUREMENTS WITH HEAT SINK

Temp °C	Conditions					Thermal Resistance(°C/W)		
	Vcb volts	Veb volts	Ic mA	Ib μA	Power mw	A	B	C
70	3.01	.725	50	710	187	126		
31	7.67	.740	50	710	420	113	168	
31	9.08	.725	50.5	670	495	114		127
31	3.03	.787	48	850	183	126		
70	3.06	.736	60	900	228	123		
31	6.92	.749	60	900	460	114	168	
31	7.93	.736	60.5	850	525	113		131
31	3.04	.797	58	1080	223	123		
70	3.06	.746	70	1050	267	124		
31	6.68	.754	70	1050	520	114	154	
31	7.20	.746	70.5	1025	560	114		133
31	3.06	.805	68	1270	263	122		
70	3.05	.755	80	1230	304	122		
31	6.22	.763	80	1230	558	114	154	
31	6.71	.755	80.5	1200	600	116		132
31	3.06	.814	77.5	1475	300	120		

Tables V and VI can be summarized as follows:

1. Readings without a heat sink are much higher than those with a heat sink indicating that the oil bath is not an infinite sink to the unit.
2. Readings by methods A and C are reasonably comparable at the higher voltages although method C gives readings somewhat higher. This may be because the junction temperature drops somewhat during the 30μsecs before the V_{BE} reading is taken. The variation of the thermal resistance with voltage by method A is not understood. It may be an inaccuracy of measurement since at low voltages we are dealing with

small junction temperature changes and it is difficult to read the change in V_{EB} accurately.

3. Readings by Method B are 40% higher than Method A. Further examination of the table will reveal this discrepancy. If we examine the readings at 3 volts at the two temperatures, the dissipations are approximately the same and so the junction temperature should differ by 39°C which is the difference of the ambients. The readings, therefore, show that V_{EB} decreases by about 1.5 mV/°C and h_{FE} increases with temperature about 0.6% per °C. Examining the readings of 3 volts and 9 volts and assuming the junction temperature to be the same, since the V_{EB}'s are the same, it is evident that h_{FE} has increased by 7%, indicating an increase in h_{FE} with V_{CB} of about 1.2% per volt. Thermal resistance has been calculated from the readings at 3 volts 70°C and 7.67 volts 31°C but the difference in V_{EB} indicates that the junction temperature is 10°C lower in the second case. The reason is that h_{FE} has increased by 5.6% due to voltage and has decreased 6% due to temperature; these two effects compensate each other to give the same I_B. If the thermal resistance is calculated, assuming the 7.67 volt reading to be 10°C lower in junction temperature

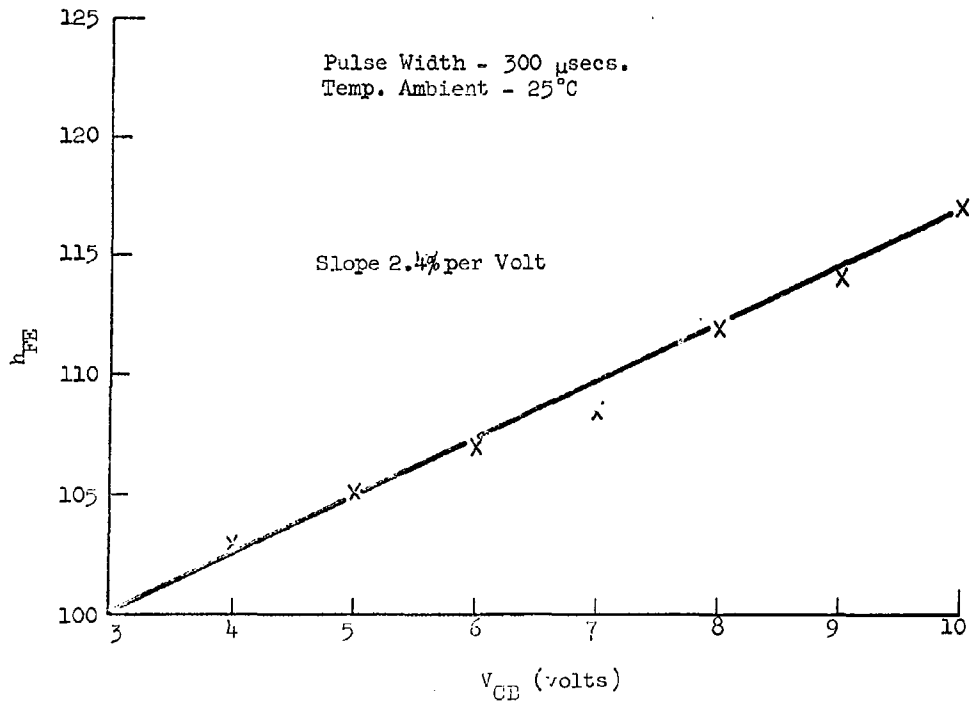
than the 3 volt 70°C reading, a new figure of 124°C/W is arrived at which is to be expected since it is based on variation of V_{EB} with temperature.

An independent check on the variation of h_{FE} with voltage and temperature is given by the results of some pulse h_{FE} measurements which are plotted in Figure 10. This shows a rise of h_{FE} with voltage of 2.4% per volt which is higher than the 1.2% deduced from Table VI, but this discrepancy is probably due to temperature rise since the pulse width is 300μsecs, and Table IV shows that there is some thermal resistance associated with this length of time.

e. Summary of Thermal Resistance Investigation - It has been shown that Methods A and C give readings within 10-15% of each other. The discrepancy may be due to the time lost in switching. As we are mainly interested in junction to air thermal resistance 10-15°C/W represents only 2-3% of the total thermal resistance.

Method B gives problems due to variation of gain with voltage and Method D has too long a switching time.

All methods except Method A have problems either with ambient or operating conditions at high stress levels and so Method A has been adopted for the investigation of junction temperature on life test.



Unit N. 7 h_{FE} normalized to its value at 3 volts

FIGURE 10 VARIATION OF h_{FE} AT 50mA WITH V_{CB}

2. Variation of Junction Temperature on Operating Life Test

a. Effects of the Ambient

The normal method of life testing devices, such as this at 25°C, is in an air temperature controlled life test chamber, with refrigeration if necessary, in order to keep the ambient under control. Unfortunately, the circulating air varies in velocity from one part of the oven to another, and this causes variations in the thermal resistance and hence, in junction temperature of the units under test, especially at high dissipation levels.

Typical variations on one device in various parts of the oven were from 303 to 390°C/W at a dissipation of 200 mw. The same device measured in a natural convection ambient at the same dissipation reads about 444°C/W.

An open rack system of life testing at room temperature was then investigated, but here again variations in thermal resistance occurred even while the device was being measured. The maximum variation in one device was 329-358°C/W at 600 mw dissipation.

A metal shield was, therefore, built to enclose 10 units on a rack. This shield enclosed a volume of 600 cubic inches of air and it reduced the variations in thermal resistance with time and position in the rack to within a few °C/W. While the ambient within this shield rises to 30°C when all ten units are operating, it remains constant throughout the volume of the shield and does not

vary with time once it has reached 30°C. This then is considered to be a satisfactory ambient in which to operate transistors at high stress levels.

During the course of the experiments it was found that thermal resistance varied with power, and this effect was further investigated. Figure 11 shows curves of variation of thermal resistance with power for 3 devices and also an average curve for four devices selected because they represented the average thermal resistance of a lot which was put up on life tests. This variation with power is considered to be the result of natural convection only, as junction to case measurements of thermal resistance show little variation with power. From the average curve Table VII was constructed assuming a thermal resistance from junction to case of 107°C/W, which is the average value, and an ambient temperature of 30°C.

TABLE VII

AVERAGE CURVE MEASUREMENTS - THERMAL RESISTANCE 107°C/W and AMBIENT TEMPERATURE 30°C

Dissipation (mw)	T_{J-A} (°C/W)	T_J (°C)	T_{J-C} (°C)	Tcase (°C)
200	500	130	21	109
300	474	172	32	140
400	455	212	43	169
500	440	250	53	197
600	428	287	64	223
700	418	323	75	248
800	409	357	86	271
900	401	391	96	295
1000	395	425	107	318

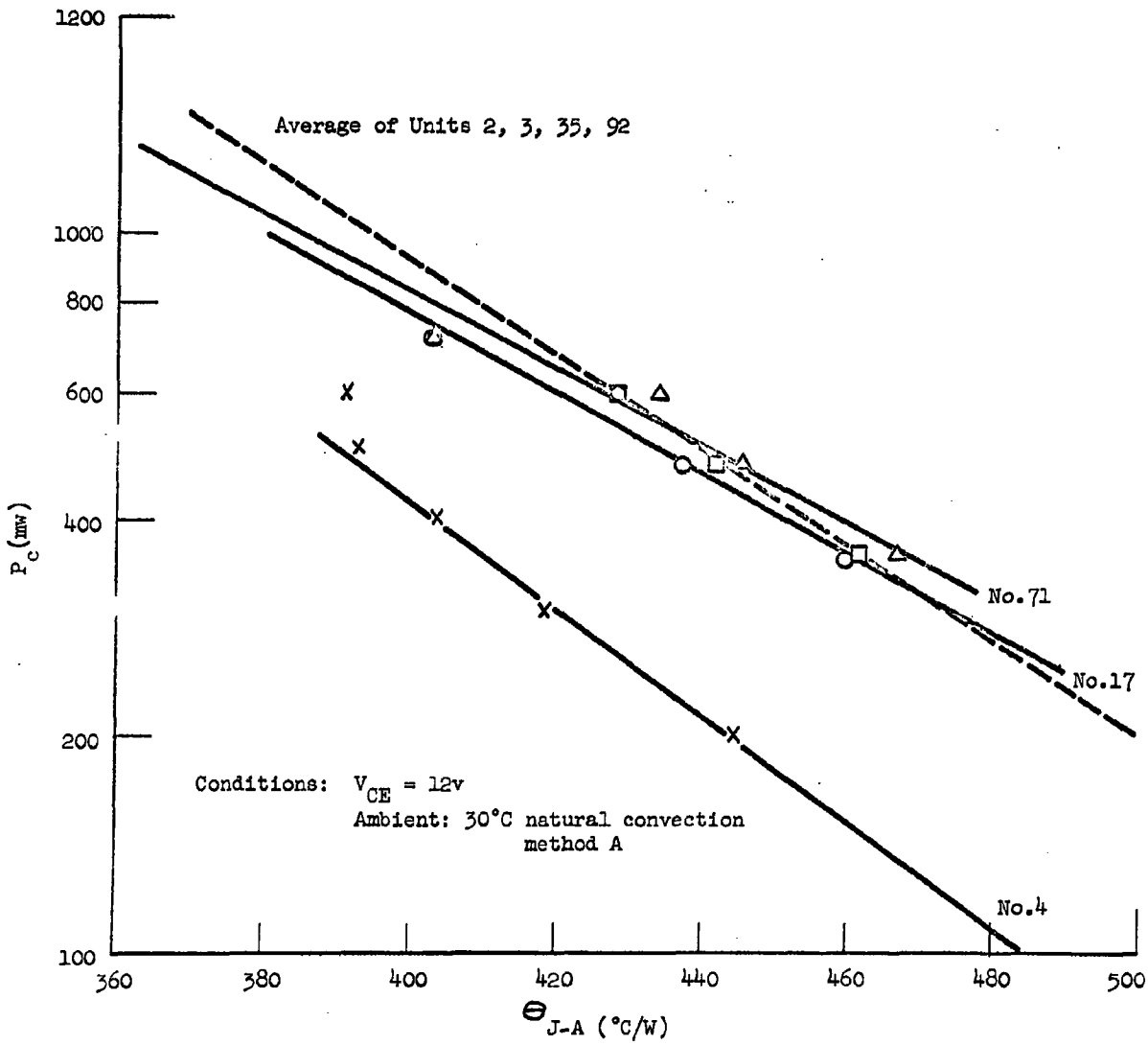


FIGURE 11 VARIATION OF THERMAL RESISTANCE WITH POWER

b. Effects of the Life Test Circuit and Transistor Parameters

The devices are run in a common base circuit with a 12 volt emitter supply voltage and an emitter resistor to define the emitter current. The collector supply is 24 volts and about half of this is dropped across the Rc. Capacitors are connected across the collector base junctions to prevent oscillations.

Variations in transistor power due to variations in the emitter resistors are to a large extent compensated for by the presence of the collector resistor, but variations in the collector resistor can cause significant variations in the power in the transistor and these resistors will be held to 1% tolerance.

The power is normally taken as $V_{CE}I_C$ which is sufficiently accurate for most purposes, but under some of the high stress conditions where the base current reverses, the emitter base voltage may also reverse. To get a true estimate of power, the emitter-base and collector-base voltages will have to be measured and multiplied by the emitter and collector currents.

The reversal of base current raises the question of whether this is a meaningful life test as the conditions are very different from those in normal operation. However, if junction temperature is the only parameter of importance and if the means by which the junction temperature is achieved do not enter into the problem, then this should provide useful data.

C. Study of Failure Rates - Extended Life Tests (A. Warren)

A study of failure rates was made using life test data on types similar to the 2N1708 produced in manufacturing. This study was considered desirable to assist in determining whether an age or burn-in processing step is necessary and/or to aid in determining acceleration factors. The failure rate study was based on the use of the Weibull Distribution as outlined in an ARINC Report.(1) A similar study is being conducted for the 2N1708 device produced as part of the reliability improvement program.

Test data chosen for this study consisted of tests with numerous down periods and in some instances ran well beyond 1000 hours. The following outline will aid in identifying the tables and figures.

300°C Life Tests - Table VIII, Figure 12

- Tables X and XII, Figures 13 and 14

360mw, 25°C Life Tests - Tables IX and XI, Figures 13 and 14

The tables show the number of failures at the various down periods. The Weibull parameters α and β are listed wherever they could be obtained.

The figures show the instantaneous failure rate. It is interesting to note that the instantaneous failure rates could only be plotted for the poorer lots since there were insufficient failures to permit a curve to be plotted for the better lots. As an aid to

(1) "Reliability of Semiconductor Devices" - Final Report - Cont. No. NObSR-81304, Dept. of the Navy, Bureau of Ships - Index No. SR0080302, St-116, dated 22 December 1961 by W.H. VonAlven and G.J.Blakmore,Jr. - ARINC Research Corporation.

analysis, "tightened limits" of $I_{CBO} > 10nA$ were used to obtain Figures 12 and 13 since there were insufficient failures at the normal end point of $I_{CBO} > 500nA$. Failure rates for the normal end points are shown in Figure 14. On one lot, identified as Lot SD, it was possible to obtain a comparison of failure rates at $I_{CBO} > 10nA$ (Figure 13) and at $I_{CBO} > 500nA$ (Figure 14). It is noted that the shape factor β is smaller for $I_{CBO} > 10nA$ than for $I_{CBO} > 500nA$, indicating that a continuing and uniform degradation of this parameter does not exist.

The failure rates on all life tests with one exception are decreasing. This would indicate that an age or burn-in could be used to remove early life failures providing that it is necessary to achieve the desired level of reliability; that it is economically justified to do so; and providing that there are no interactions as discussed in the next section. (Section VE)

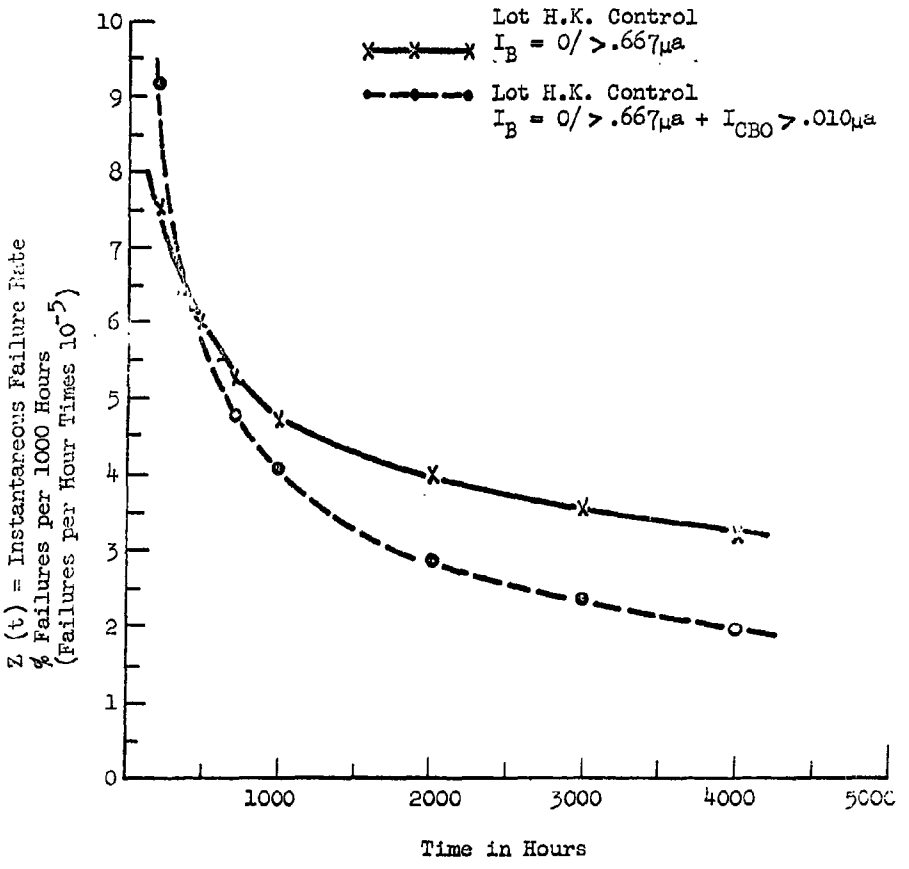


FIGURE 12 FAILURE RATE CURVES FOR 300°C SHELF LIFE TEST

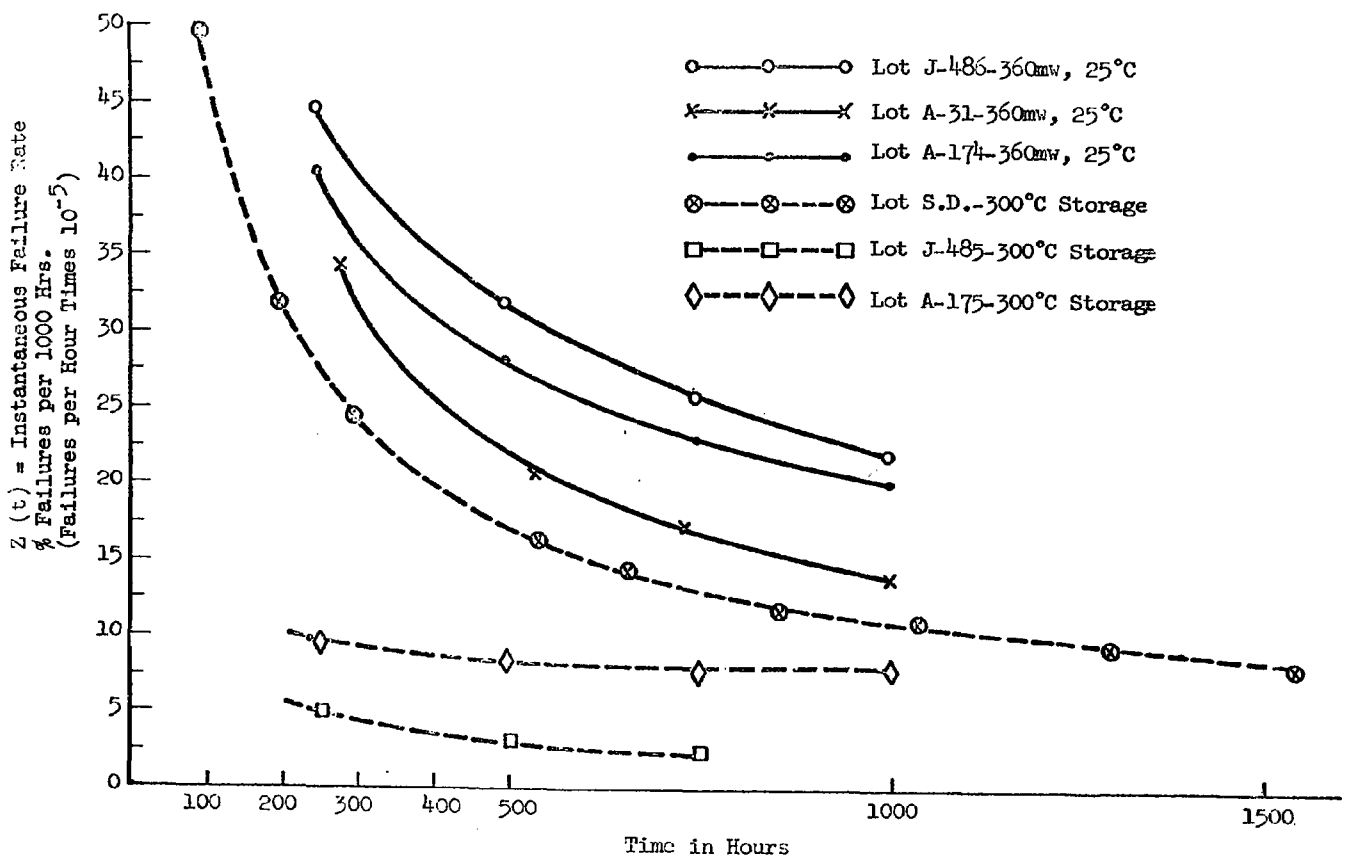


FIGURE 13 FAILURE RATE CURVES - $I_{CBO} > .010\mu a$

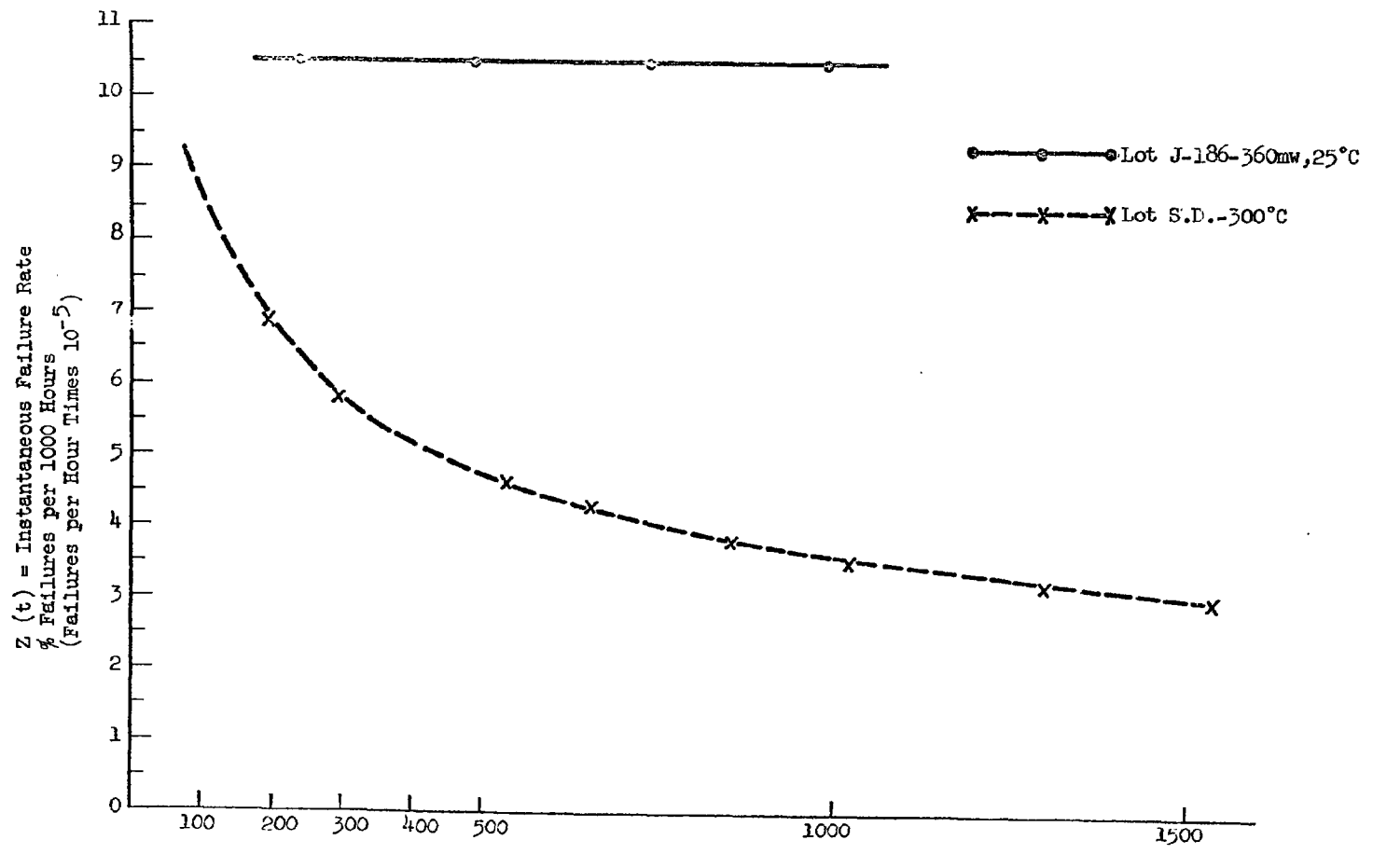


FIGURE 14 FAILURE RATE CURVES - $I_{CBO} > .500\mu a$

TABLE VIII

300°C LIFE TESTS

Lot Identification: HK Test+

Condition: Thinner Aluminum

Sample Size: 67 Units

Characteristic	Hours and Failures per Sample											Weibull Parameters	
	0	200	483	723	1018	2054	3014	4030	5009	5994	8015	α	β
$I_{CBO} > .010\mu a$	1/67	1/66	0/65	0/65	0/65	0/65	0/65	1/65	0/64	0/64	0/64	-	-
$I_{CBO} > .500\mu a$	No Failures →											-	-
$I_B = 0/>.667\mu a$	2/67	No Failures →										-	-
TOTAL $I_{CBO}>.010\mu A$ $I_B=0/>.667\mu a$	3/67	1/64	0/63	0/63	0/63	0/63	0/63	1/63	0/62	0/62	0/62	-	-

Lot Identification: HK Control+

Condition: Thicker Aluminum

Sample Size: 70 Units

Characteristic	Hours and Failures per Sample											Weibull Parameters	
	0	200	483	723	1018	2054	3014	4030	5009	5994	8015	α	β
$I_{CBO} > .010\mu a$	0/70	2/70	2/68	1/66	0/65	0/65	0/65	0/65	0/65	0/65	0/65	-	-
$I_{CBO} > .500\mu a$	0/70	1/70	2/69	1/67	0/66	0/66	0/66	0/66	0/66	0/66	0/66	-	-
$I_B=0/.667\mu a$	5/70	1/65	2/64	1/62	0/61	2/61	2/59	1/57	0/56	0/56	0/56	14.9	.72
TOTAL $I_{CBO}>.010\mu A$ $I_B=0/>.667\mu a$	5/70	3/65	4/62	2/58	0/56	2/56	2/54	1/52	0/51	0/51	0/51	12.2	.5

+ See Coded Eng. Ltr 929-3 by H. Khajezadeh

TABLE IX

360mw .25°C LIFE TESTS - WITH AND WITHOUT 500 HR. TEMPERATURE AGE

Lot Identification: H-403 - 33rd Week

Condition: 300°C Temperature Age, 96 Hrs.

Sample Size: 110 Units

Characteristic	Hours and Failures per Sample				Weibull Parameters	
	0	530	986	Total Failures	α	β
$I_{CBO} > .010\mu a$	1/110	6/109	1/103	8/110	-	-
$I_{CBO} > .500\mu a$	No	Failures →			-	-
$I_B = 0/> .667\mu a$	No	Failures →				

Lot Identification: A-31 - 33rd Week

Condition: 300°C Temperature Age, 96 Hours and 500 Hours

Sample Size - 110 Units

Characteristic	Hours and Failures per Sample						Weibull Parameters	
	0	285	546	736	994	Total Failures	α	β
$I_{CBO} > .010\mu a$	1/110	29/109	7/80	0/73	3/73	40/110	2.12	0.3
$I_{CBO} > .500\mu a$	0/110	2/110	1/108	0/107	0/107	3/110	-	-
$I_B = 0/> .667\mu a$	No Failures →						-	-

TABLE X

300°C LIFE TESTS - SAMPLES FROM 33rd WEEK

Lot Identification: H-402 - 33rd Week

Condition: Temperature Age, 96 Hrs.

Sample Size - 110 Units

Characteristic	Hours and Failures per Sample				Weibull Parameters	
	0	869	1012	Total Failures	α	β
$I_{CBO} > .010\mu a$	3/110	9/107	0/98	12/110	-	-
$I_{CBO} > .500\mu a$	0/110	1/110	0/109	1/110	-	-
$I_B = 0/> .667\mu a$	No Failures →				-	-

Lot Identification: SD- 33rd Week

Condition: 300°C - Temperature Age, 96 Hrs.

Sample Size: 150 Units

Characteristic	Hours and Failures per Sample											Weibull Parameters	
	0	100	200	300	540	662	865	1036	1300	1540	Total Failures	α	β
$I_{CBO} > .010\mu a$	6/150	17/144	7/127	2/120	6/118	1/112	2/111	2/109	1/107	3/106	47/150	3.1	0.35
$I_{CBO} > .500\mu a$	0/150	0/150	4/150	0/146	1/146	1/145	3/144	1/141	0/140	1/140	11/150	16.5	0.6
$I_B = 0/> .667\mu a$	No Failures →											-	-

TABLE XI

360mw, 25°C LIFE TESTS - WITH AND WITHOUT 500 Hr. TEMPERATURE AGE

Lot Identification: J-486 - 43rd Week

Condition - 300°C Temperature Age, 96 Hrs.

Sample Size - 110 Units

Characteristic	Hours and Failures per Sample						Weibull Parameters	
	0	250	500	750	1000	Total Failures	α	β
$I_{CBO} > .010$ μa	0/110	24/110	7/86	1/79	12/78	44/110	2.23	0.5
$I_{CBO} > .500$ μa	0/110	3/110	4/107	1/103	3/100	11/110	9.49	1.0
$I_B = 0/> .667$ μa	No Failures →						-	-

Lot Identification: A-174 - 43rd Week

Condition- 300°C Temperature Age 96 Hours and 500 Hours

Sample Size - 110 Units

Characteristic	Hours and Failures per Sample						Weibull Parameters	
	0	250	500	750	1000	Total Fialures	α	β
$I_{CBO} > .010$ μa	0/110	21/110	10/89	1/79	8/78	40/110	8.1	0.5
$I_{CBO} > .500$ μa	0/110	3/110	0/107	0/107	2/107	5/110	-	-
$I_B = 0/> .667$μa	No Failures →						-	-

TABLE XII

300°C LIFE TESTS - SAMPLES FROM 43rd WEEK

Lot Identification: J-485 - 43rd Week
Condition: 300°C Temperature Age, 96 Hours
Sample Size - 110 Units

Characteristic	Hours and Failures per Sample					Weibull Parameters	
	0	250	500	750	Total Failures	α	β
$I_{CBO} > .010\mu a$	0/110	3/110	1/107	1/106	5/110	19.1	0.4
$I_{CBO} > .500\mu a$	0/110	3/110	0/107	0/107	3/110	-	-
$I_B = 0/> .667\mu a$	No Failures →					-	-

Lot Identification: A-175-43rd Week
Condition: 300°C Temperature Age, 96 Hours
Sample Size - 110 Units

Characteristic	Hours and Failures per Sample						Weibull Parameters	
	0	250	500	750	1000	Total Failures	α	β
$I_{CBO} > .010\mu a$	0/110	3/110	2/107	2/105	3/103	10/110	11.1	0.9
$I_{CBO} > .500\mu a$	0/110	3/110	0/107	0/107	0/107	3/110	-	-
$I_B = 0/> .667\mu a$	No Failures →						-	-

D. The Effect of Variations of I_C and V_{CB} on 300 mw Operating Life Tests (F.Wehrfritz)

Tests have been performed on experimental lots AE, AF, AG and PF. Units have been operated at 300 mw, 25°C in the air temperature controlled life test chambers at V_{CB} = 15, 12 and 6 volts for 1000 hours. Approximately 20 units were tested at each voltage. The experimental lots represent four processing variations which were under investigation.

No changes have taken place in the parameters over the 1000 hours observation period from the initial readings. No differences are noted at this power level for the three voltages. Table XIII is a summary of the results which includes the median and range of values for the four lots.

E. A Study of the Effect of 300°C Temperature Aging on 300 mw Operating Life Tests (F.Wehrfritz, S.Dansky, A.Warren)

In Section C it was established that the failure rates are normally decreasing for 300°C storage life tests and 300 mw, 25°C operating life tests. This would indicate that a prestressing of the units under the same condition as the life tests would reduce the number of early-life failures in the life test. However, it does not consider interactions which may occur. In an effort to evaluate one possible interaction, it was decided to study the effect of 300°C temperature aging on operating life tests.

Several experiments were performed as follows:

1. A test was performed on samples from two lots of factory product, similar to the 2N1708. The units

TABLE XIII

RESULTS-CONSTANT POWER TESTS
AT 300mw - AT 15,12,6 VOLTS-1000 HOURS

Lot No.	Volts	I_{CBO} Median	I_{CBO} Range	h_{FE} Median	h_{FE} Range	Remarks
AE	15	.003	.002-.004	20	14-29	No Change
	12	.003	.002-.006	23	17-29	0-1000 Hours
	6	.003	.002-.006	23	14-26	
AF	15	.003	.003-.008	56	44-77	No Change
	12	.003	.003-.004	59	41-71	0-1000 Hours
	6	.003	.003-.004	56	41-77	
PF	15	.002	.002-.004	53	38-99	No Change
	12	.002	.001-.004	53	31-99	0-1000 Hours
	6	.002	.001-.003	65+	29-99	+ 5% >99
AG	15	.003	.002-.003	65	41-99	No Change
	12	.003	.002-.003	59	43-79	0-1000 Hours
	6	.003	.002-.003	59	41-98	

were subjected to a 300°C temperature age for 500 hours. Characteristics of these units which should be noted are:

a. Units were sealed in a T018 case rather than a T046 case as used on the 2N1708.

b. Units were processed with aluminum contacts, gold lead wire and an encapsulant.

The units were subjected to 360 mw at 25°C in air-cooled chambers for 1000 hours. On one lot a significant I_{CBO} degradation occurred on test units which were subjected to the temperature age in comparison to control units which were not subjected to the temperature age. (Refer to Table IX, Section VC on Failure Rates). On a second lot no significant difference was noted for $I_{CBO} > 0.010\mu A$ while the opposite effect was noted for $I_{CBO} > 0.500\mu A$ (Refer to Table XI, Section VC). However, the number of failures were excessively high on both test and control indicating this lot was not representative of the process. It is believed that the first test indicates that a 300°C - 500 hour temperature age will degrade at least certain lots of product on subsequent 360 mw, 25°C operating life tests. These results are similar to those that might be expected on 2N1708 units in a T046 case at 300 mw, 25°C.

2. A test was performed on 2N1708 units processed using two different types of contacts - gold (Lot AE) and aluminum (Lot AG). Units were processed in both cases without an encapsulant and were subjected to a 300°C

temperature age for 96 hours.

The data in Table XIV indicates the failures which developed in temperature aged units from lots AE and AG while on 300 mw (15V) life test. Failures, defined as I_{CBO} greater than 10 nA, and $I_B > .667 mA/0$ occurred on aged units. No failures, similarly defined, have been observed at 1000 hours in units which were not aged.

TABLE XIV

TEMPERATURE AGED FAILURES ON 300 mw (15V) LIFE TEST

Lot No.	Parameter	Hours on Test						
		0	24	50	96	256	514	1012
AE	I_B	0	0	2	2	2	2	2
n=15	I_{CBO} >10nA	1	1	1	3	3	3	3
	I_{CBO} >500nA	0	0	0	0	0	0	0
		0	22	43	131	219	505	1006
AG	I_B	0	0	0	0	0	0	0
n=20	I_{CBO} >10nA	1	2	2	2	2	3	4
	I_{CBO} >500nA	0	0	0	0	0	0	0

Based on the data presented, it can be stated that a 300°C temperature age for 96 hours will degrade units on subsequent 300 mw, 25°C operating life tests when units are processed without an encapsulant. The effect on units processed with an encapsulant cannot be positively stated. However, consideration of this data combined with the results described previously in

this section indicate that a temperature age should not be used without further investigation for a 2N1708 high reliability unit.

F. Study of Variables Data on Accelerated Life Test at Various Down Periods (F.Tumbelty)

Variables data in this program are used for two separate and distinct purposes. First, to evaluate each individual unit through respective down periods (Figure 15, I_{CBO}). Examples: unit 2 read .005μa at zero hours and $>$ .500μa after 48 hours; unit 33 left the I_{CBO} distribution at the 96 hour down period and returned to the distribution after 96 hours; and unit 19 left the I_{CBO} distribution at the 48 hour down period but did not progressively deteriorate in subsequent down periods.

Secondly, to evaluate the stability of distributions by lot, stress and down period in a condensed form. Notice in Figures 16 and 17 , lot AG deteriorated faster at 340°C than did lot PF for I_{CBO} and h_{FE}. Lot AG was not as stable as lot PF at 200°C for h_{FE} (Figures 18 and 19 200°C). Lot PG (Figure 20) at 300°C was more stable with the encapsulant after 500 hours of life for I_{CBO}.

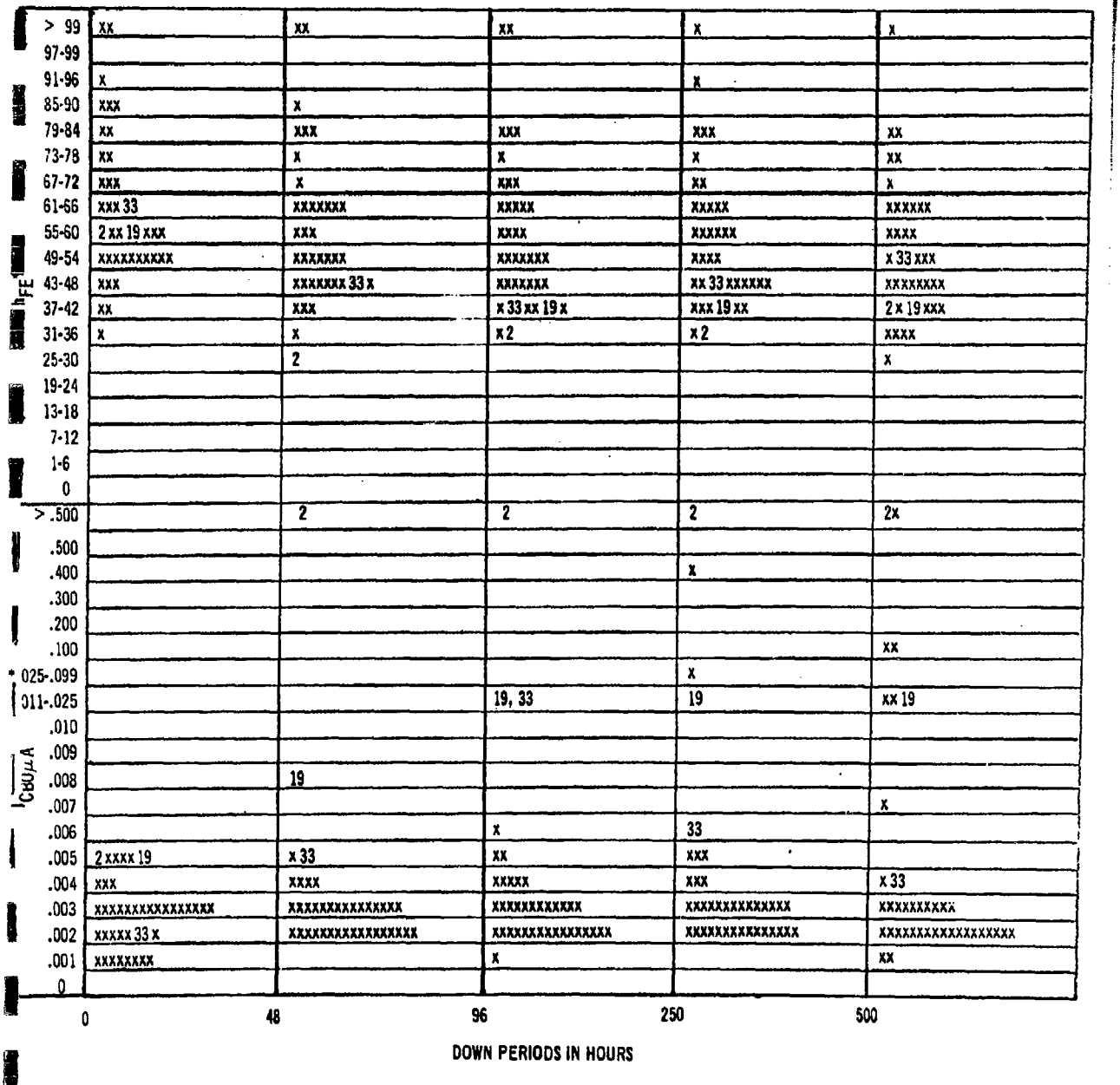
There are revealing conclusions drawn from variables data which are not apparent when evaluating attribute data. One of the most significant variables data contributions is a comparison of temperatures in the 300°C range. I_{CBO} distributions tend to remain stable through

time; however, individual units suddenly leave the distributions. It is interesting to note that it is impossible to judge a unit a potential failure because it leaves the distribution. On the other hand, units that do become failures are not necessarily unstable units at previous down periods. It seems impossible to predict failures from prior data.

Applying stresses greater than 300°C, h_{FE} distributions hold together longer than I_{CBO} distribution. In comparing 90th, 50th, and 10th percentiles, I_{CBO} percentiles reach life end points before similar h_{FE} percentiles. This establishes the fact that most units initially fail for I_{CBO}.

Distributions of I_{CBO} and h_{FE} have limited variance in time and 300mw operating life and 200°C shelf life tests. It is rare for units stressed at 300 mw or 200°C to exceed an I_{CBO} of .010μa or for h_{FE} to approach 15. There have been no distribution fluctuations for 2000 hours of life.

Another interesting point to note is the variables data comparing encapsulant versus no encapsulant. Any temperature stress above 260°C will show more stable I_{CBO} distributions with the use of the encapsulant.



* LARGER CELL SIZE USED

FIGURE 15 EXAMPLE OF LOT PF AT 320°C

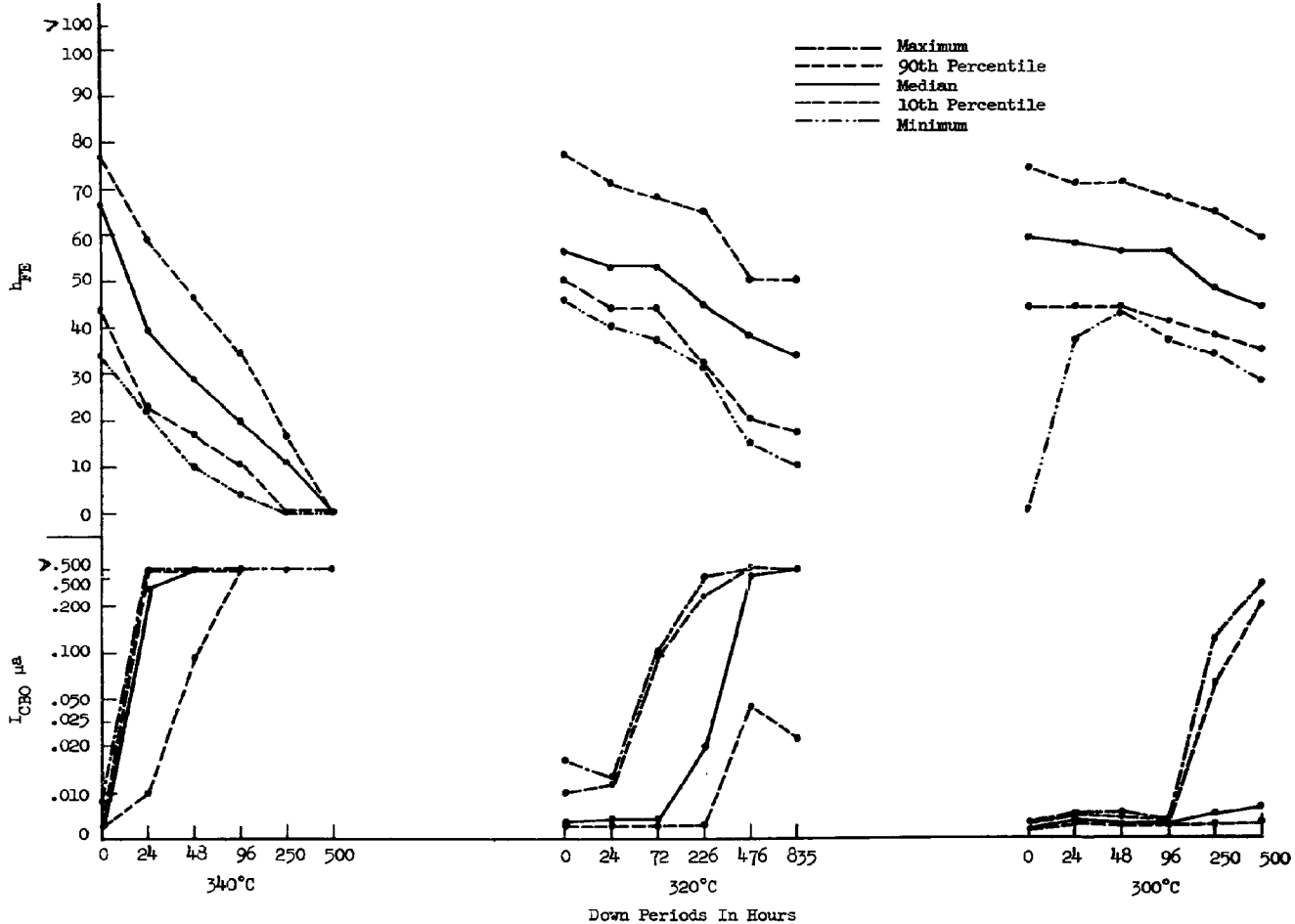


FIGURE 16 I_{CBO} AND h_{FE} DISTRIBUTIONS THROUGH RESPECTIVE DOWN PERIODS BY STRESS - LOT AG (SHELF)

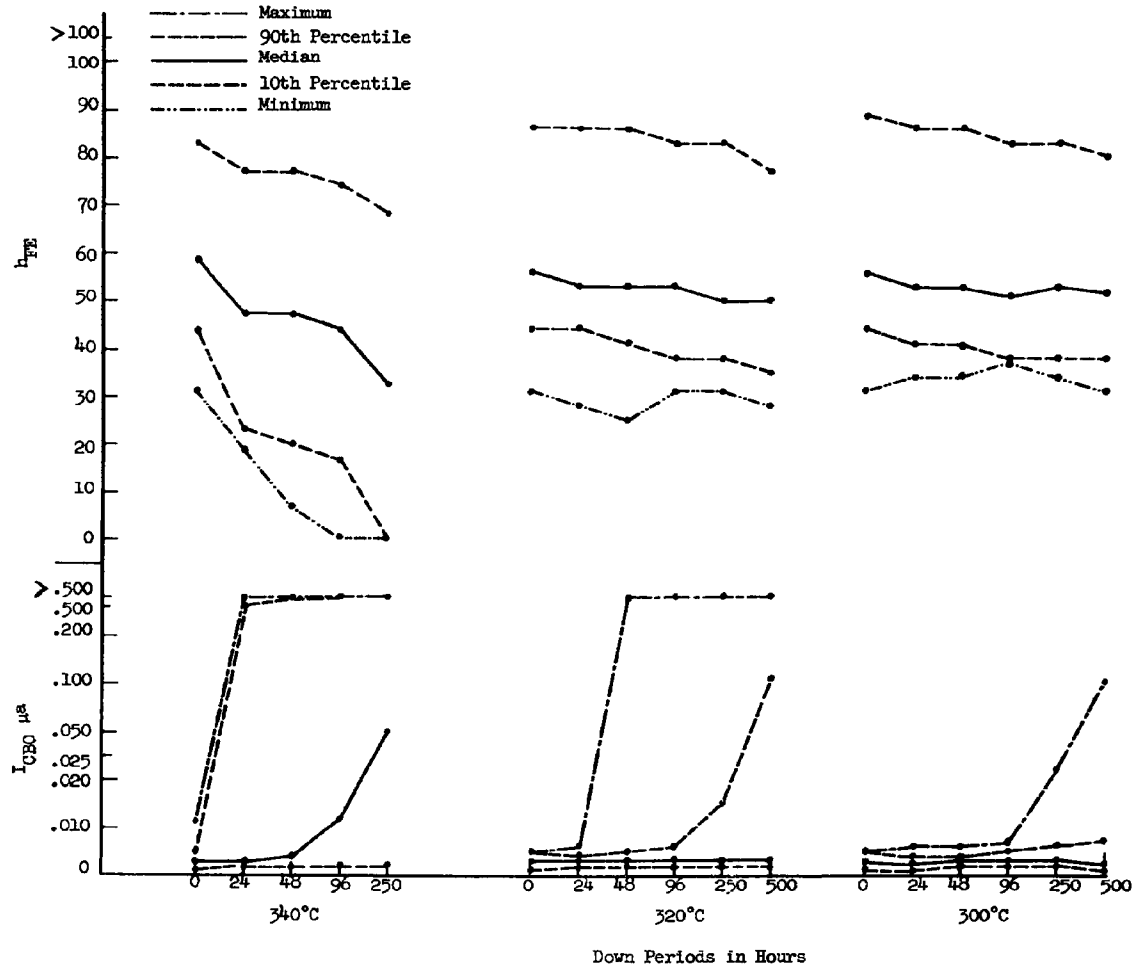


FIGURE 17 I_{CBO} AND h_{FE} DISTRIBUTIONS THROUGH RESPECTIVE DOWN PERIODS BY STRESS - LOT PF (SHELF)

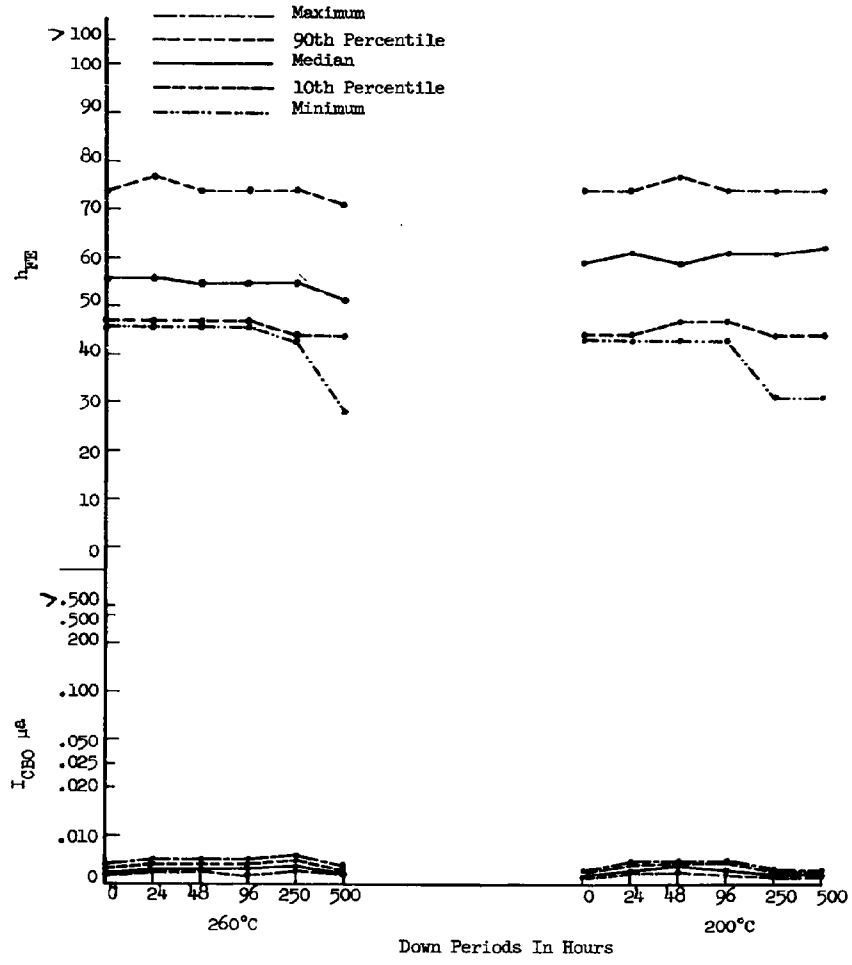


FIGURE 18 I_{CBO} AND h_{FE} DISTRIBUTIONS THROUGH RESPECTIVE DOWN PERIODS BY STRESS - LOT AG (SHELF)

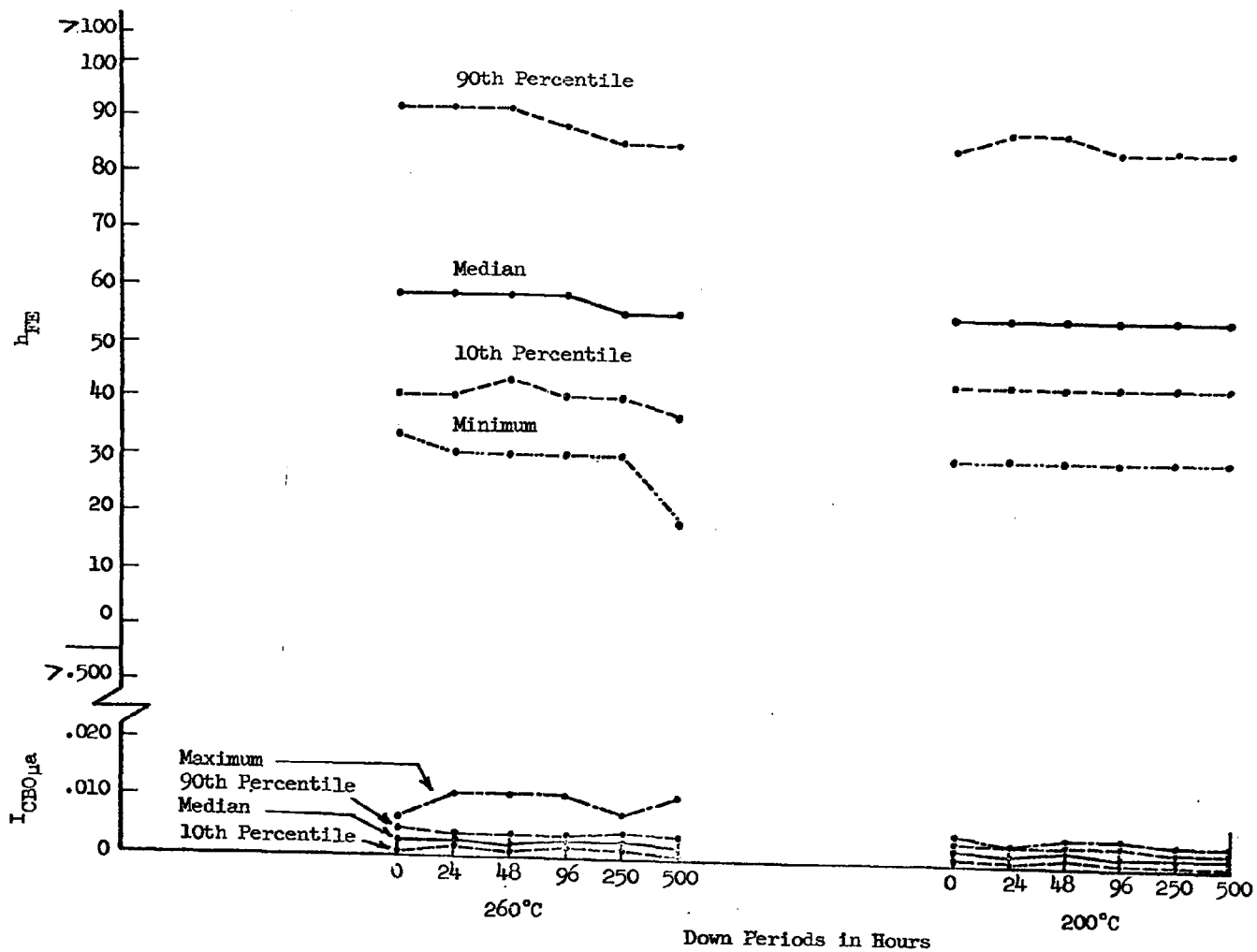


FIGURE 19 LOT PF (SHELF) AT 200°C

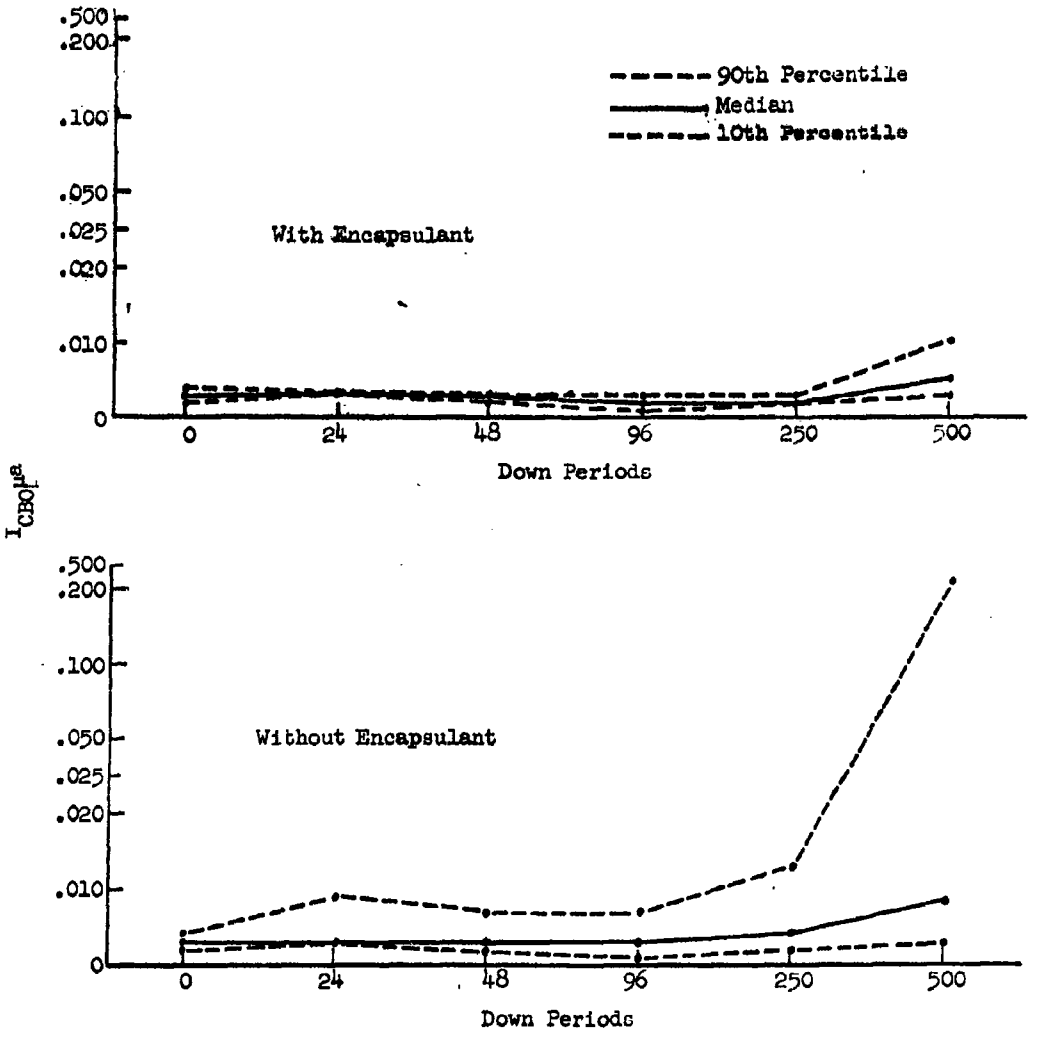


FIGURE 20 LOT PG AT 300°C

G. A Discussion of the Use of Power-Step-Stress Tests to Evaluate Process Changes (F. Wehrfritz, W. Totten)

Power-step-stress tests have been used in an attempt to evaluate processing experiments in an expeditious manner. Such tests were reported in the First and Second Quarterly Reports. Two series of additional tests have been run as described below.

1. First Series

A comparison was made of four lots, designated as AE, AF, AG and PF, representing different process variations. Approximately 20 units were selected from each lot. The results obtained are shown in Tables XV and XVI.

The tests were performed in the temperature controlled life test chambers. Test cards and circuits were developed and applied at the following milliwatt power levels: 300, 350, 400, 450, 545, 660, 760, 785, 815, 855, 885, 920 and 950. The procedure used consisted of applying power for one hour, allowing the units to come to equilibrium for 30 minutes and then measuring BV_{EBO}, BV_{CBO}, V_{CE}, V_{BE}, I_B and I_{CBO}. Failures were defined as collector-to-emitter shorts, emitter or collector shorts, I_{CBO} = 11 na to 500 na or $I_{CBO} > 500$ na and $I_B > .667$ ma.

A tabulation of failures, which shows the points and causes of failure, is shown in Tables XV and XVI. A study of these tables makes some of the advantages and limitations of step-stress testing readily apparent.

a. For step-stress tests to be meaningful in predicting performance under normal operating conditions, the types of failures detected must be the same as those which occur under

normal operating conditions. Tables XV and XVI indicate that most of the units fail as a result of shorts at 760 mw or above. Failures due to shorts have not been observed under normal operating conditions. It is believed that failures of this type represent limitations of the device design and it is very unlikely that the failures would occur under normal operating conditions. Therefore, in evaluating the various processes represented by these tests these failures were not considered.

b. The "opens" observed on Lot AE are considered representative of failures which may occur under normal operation conditions. Failures of this type have not been observed on 300 mw (25°C) operating life in 1000 hours, however, such failures may eventually occur on units produced by this process. "Opens" have been observed on high constant temperature life tests.

c. The high I_{CBO} values obtained on lot PF at lower steps are considered representative of this particular process. Since such "failures" do occur under normal operating conditions, tighter I_{CBO} limits (10 na) had to be employed to observe this effect.

2. Second Series

Tests were performed as described above on five lots designated as PG-1, PG-2, AH, AK-1 and AK-2. The results obtained are shown

in Tables XVII, XVIII and XIX.

In an attempt to minimize the significance of the position occupied by devices on the circuit card, a"latin square" physical arrangement of the units was utilized. (A discussion of the variation in thermal resistance in the air-cooled life test chambers is given in Section V-B).

Additional observations may be made regarding the use of step-stress tests by referring to Tables XVII, XVIII and XIX. The observations made would include:

a. The comments made on shorts in Section VA are applicable to these tests.

b. There is no apparent difference between the test and control represented by samples from Lots PG-1 and PG-2 (Table XVII).

c. The units used to comprise samples from Lot AK-1 and AK-2 (Table XVIII) constituted inferior product since initial I_{CBO} readings were greater than 10 na. However, three important observations may be made: a) If an I_{CBO} failure criteria of 500 na is used, it becomes apparent that AK-2 was initially inferior to AK-1; b) Units from AK-2 and AK-1 recovered (returned to initial values) as stress was increased. It should be noted that observations made under normal operating conditions have confirmed that the initial degradation and recovery is indicative of the processes represented by these lots; c) All units tested satisfactorily at 1 watt. This was the highest power level achieved on any test, without the occurrence of shorts.

Since these units represent a design change which would improve power capabilities, the results obtained are meaningful.

d. It is interesting to note that similar behavior, with regards to an initial I_{CBO} degradation and recovery, may be observed on Lot AH (Table XIX) as occurred on Lot AK (Table XVIII). These effects were produced by a similar process variation.

Based on the above analysis, one may conclude that power-step-stress testing is a significant tool for rapid evaluation of process improvements, providing that the cause of failure is carefully analyzed and related to what may occur under normal life test conditions.

TABLE XV

RESULTS OF STEP-STRESS TESTS MADE ON LOTS AE AND AF

Lot No.	Unit No.	Step-Stress Power Levels (mw)											
		350	400	450	545	660	760	785	815	855	885	920	950
AE	61							SE					
	62						SE						
	63						SE						
	64											J	
	65												
	66											S	
	67								SE				
	68								S				
	69								S				
	70								SE				
	71											S	
	72								SE				
	73							O					
	74								S				
	75								S				
	76											G	
	77											S	
	78							O					
	79							O					
	80							SE					
AF	61											G	
	62										S		
	63											G	
	64										S		
	65											G	
	66											G	
	67										S		
	68									S			
	69										S		
	70										S		
	71										S		
	72										I_b	O	
	73										S		
	74											G	
	75										S		
	76											G	
	77					>10	>10	>10	>10	>10	>10	>10	
	78												
	79										S		
	80											G	

Symbol	Description	Symbol	Description
>10	$I_{CBO}(V_{CB}=15V)$ = 11nA-500nA	SE	Emitter Short
>500	$I_{CBO}(V_{CB}=15V)$ = 50nA	O	Open
I_b	$I_b > .667$	G	Good
S	Collector-to-Emitter Short		

NOTE: Units are removed from test if they reveal shorts or opens, otherwise they are tested at each step as shown.

TABLE XVI

RESULTS OF STEP-STRESS TESTS MADE ON LOTS AG AND PF

Lot No.	Unit No.	Step Stress Power Levels (mw)											
		350	400	450	545	660	760	785	815	855	885	920	950
AG	81									S			
	82								S				
	83								S				
	84								S				
	85								S				
	86										G		
	87							>10	S				
	88									S			
	89								S				
	90								S				
	91										S		
	92										S		
	93										S		
	94										S		
	95										S		
	96								S				
	97										S		
	98										S		
	99								S				
	100										S		
PF	1											G	
	2								S				
	3								S				
	4									S			
	5											G	
	6					>10	>10	>10	>10	>10	S		
	7	>10	>10	>10							S		
	8								S				
	9					>10	>10		>10			S	
	10				>10	>10	>10		S				
	11				>10	>10	>10	>10	>10	>10	S		
	12								S				
	13											G	
	14									>10	S		
	15								S				
	16												
	17											S	
	18					>10	>10	>10	>10	>10	S		
	19										S		
	20							>10	S				

Symbol	Description	Symbol	Description
>10	$I_{CBO}(V_{CB}=15V)$ = 11nA to 50nA	S	Collector-emitter Short
>500	$I_{CBO}(V_{CB}=15V)$ = 500nA	SE	Emitter Short
I_b	$I_b(I_c=10mH, V_{CE}=1V) > .667$	O	Opens
		G	Good

NOTE: Units are removed from test if they reveal shorts or opens, otherwise they are tested at each step as shown.

TABLE XVII

RESULTS OF STEP-STRESS TESTS MADE ON LOTS PG-1 AND PG-2

Lot No.	Unit No.	Step Stress Power Levels (mw)													
		293	351	444	545	660	695	760	785	815	855	885	920	950	1000
PG-1	1										S				
	7												>500	-	
	13									S					
	19										S				
	25									S					
	26									S					
	32									S					
	38									S					
	44									S					
	50							S							
	51												S		
	57									S					
	63									S					
	69									S					
	75									S					
	76									S					
	82									S					
	88										S				
	94									S					
	100							S							
PG-2	2										I_b	S			
	8												S		
	14									S					
	20									S					
	21									S					
	27								>10	S					
	33									S					
	39												S		
	45									S					
	46									S					
	52											S			
	58									S					
	64										I_b	I_b	S		
	70									S					
	71										>500	S			
	77									S					
	83										>500				
	89								S						
	95									S					
	96										>500				

Symbol	Description	Symbol	Description
>10	$I_{CBO}(V_{CB}=15V)$ = 11nA-500nA	SE	Emitter Short
>500	$I_{CBO}(V_{CB}=15V)$ = 50nA	O	Open
I_b	$I_b > .667$	G	Good
S	Collector-to-Emitter Short		

NOTE: Units are removed from test if they reveal shorts or opens, otherwise they are tested at each step as shown.

TABLE XVIII

RESULTS OF STEP STRESS TESTS MADE ON LOTS AK-2 AND AK-1

Lot No.	Unit No.	Step Stress Power Levels (mw)													
		293	351	444	545	660	695	760	785	815	855	885	920	950	1000
AK-2	5		>500												G >10
	6				>500										G >10
	12				>500										G >10
	18			>500											G >10
	24							All units >10 unless							G >10
	30		>500					otherwise noted. All							G >10
	31			>500				units recovered and returned							G >10
	37							to initial values as stresses							G >10
	43			>500				increased							G >10
	49			>500											G >10
	55			>500											G >10
	56			>500			>500								G >10
	62														G >10
	68				>500										G >10
	74			>500											G >10
	80		>500	>500			>500			>500					G >10
	81			>500											G >10
	87			>500		>500									G >10
	93				>500										G >10
	99			>500											G >10
AK-1	4					>500			All units >10 unless						G >10
	10						>500		otherwise noted. All						-
	11								units recovered and						G >10
	17						>500		returned to initial values						G >10
	23								stresses increased						G >10
	29						>500								G >10
	35										>500				G >10
	36											>500			G >10
	42									>500					-
	48														G >10
	54													>500	G >10
	60									>500					G >10
	61														G >10
	67														G >10
	73				>500										G >10
	79														G >10
	85														G >10
	86										>500				G >10
	92									S					
	98									>500					G >10

Symbol	Description	Symbol	Description
>10	$I_{CBO}(V_{CB}=15V)$ = 11nA-500nA	SE	Emitter Short
>500	$I_{CBO}(V_{CB}=15V)$ = 50nA	O	Open
I_b	$I_b > .667$	G	Good
S	Collector-to-Emitter Short		

NOTE: Units are removed from test if they reveal shorts or opens, otherwise they are tested at each step as shown.

TABLE XIX

RESULTS OF STEP-STRESS TESTS ON LOT AH

Lot No.	Unit No.	Step Stress Power Levels (mw)													
		293	351	444	545	660	695	760	785	815	855	885	920	950	1000
AH	3											S			
	9												S		
	15				>10	>10	>10					I_b	S		
	16				>10	>500	>10						S		
	22										S				
	28			>500	>500	>10	>10			S					
	34				>10					>500					
	40											S			
	41				>10	>10	>10	>10						>500	
	47											S			
	53				>10	>10	>10					S			
	59			>500	>10	>10	>10						S		
	65				>10	>10						>500			
	66						>10	>10						S	
	72									S					
	78				>10					S					
	84				>10					S					
	90			>10	>10					>500					
	91											I_b	>500		
	97				>10	>10	>10			S					

Symbol	Description	Symbol	Description
>10	$I_{CBO}(V_{CB}=15V)$ = 11nA-500nA	SE	Emitter Short
>500	$I_{CBO}(V_{CB}=15V)$ = 50nA	O	Open
I_b	$I_b > .667$	G	Good
S	Collector-to-Emitter Short		

NOTE: Units are removed from test if they reveal shorts or opens, otherwise they are tested at each step as shown.

VI. CONCLUSIONS

A. Process Improvements

Process improvements have been completed in all areas investigated in this program. Those areas completed during the present report period are as follows:

1. Photoresist and Etching Technique

   An improved method of removing photoresist has been developed. Other process improvements have also been effected.

2. Surface Preparation and Cleaning

   A study of inorganic reagent materials as sources of semiconductor surface contamination was completed. Conclusions concerning the concentrations of impurities and the effectiveness of various desorption techniques are included in the text of the report.

3. Contact Preparation

   The use of thin aluminum contacts has inhibited formation of "purple plague". Experiments with gold contacts were unsuccessful.

4. Bonding

   The use of an encapsulant will improve bond strength after high temperature testing. The use of gold alloy wire did not materially improve the bond strength. Nailhead bonding with a smaller diameter gold wire to reduce the size of the ball met with only limited success due to difficulties of keeping the ball within the required area.

5. Sealing

There is a significant reduction in failure rate on high temperature life tests when an encapsulant is used. An improvement in operating life performance has been achieved through the use of a pure grade of material. The use of various types of dessicants has not reduced the failure rate on high temperature tests.

6. Ceramic Stem

A glass to metal stem has been developed for use in the program. Although encouraging results have been obtained in efforts to produce the ceramic stem, it is not to the best interests of the program to incorporate this stem into the program at this time.

B. Reliability Testing and Analysis

A program of reliability testing and analysis has been completed.

1. Acceleration curves for high temperature shelf life tests have been developed. These curves indicate extremely large acceleration factors for the process adopted in this program.
2. Studies of thermal resistance measurements from junction to ambient (T_{J-A}) have been completed.
   a. T_{J-A} measurements made using V_{EB} as the temperature sensitive parameter at I_E = 1 mA with the collector circuit open have advantages over three other methods evaluated.
   b. T_{J-A} measurements are considerably higher under natural convection conditions than under circulating air conditions at supposedly the same ambient temperature.

c. T_{J-A} varies with power dissipation.

d. T_{J-A} variation on one device in various parts of the air temperature controlled life test chambers is very large.

e. T_{J-A} variation between devices is very large.

f. Variations in the collector resistor in the life test circuit can cause significant variations in power in the transistor.

g. Under very high power conditions the base current reverses direction. The significance of life tests run under these conditions is questionable.

3. A study of failure rates on types similar to the 2N1708 has shown that the failure rate for high temperatures shelf and operating life tests is normally decreasing.

4. Operating life tests performed at 300 mw, 25°C on samples from experimental lots of 2N1708 devices have not shown a significant difference in parameters investigated between V_{CB} = 15, 12 and 6 volts after 1000 hours.

5. A temperature age at 300°C to pre-stress units to permit removal of potential life failures should not be used without further investigation because of indications of the detrimental effect on operating life tests.

6. A study of variables data is an essential tool in reliability analysis.

7. Power step stress tests provide a rapid method of evaluating the effect of process changes on operating life tests.

VII. PROGRAM FOR NEXT INTERVAL

The production run to demonstrate the reliability level achieved as a result of the process improvements effected is in operation and will continue through the next interval. Reliability testing and analysis of production lots will be performed with particular emphasis on establishing acceleration factors.

VIII. PERSONNEL AND MAN-HOURS

The personnel contributing to the program during this quarter are listed in Table XX. Figure 21 depicts the 2N1708 Reliability Improvement Project Organization.

TABLE XX

MANHOURS FOR THE FOURTH QUARTER

Name	February	March	April	Total
		ENGINEERS		
W.L. Totten	160	168	160	488
G.F. Granger	160	168	160	488
A.A. Dunham	15	25	20	60
J.F. Vance	25	40	60	125
P.J. Grenier	160	168	160	488
W.M. Triggs	31	3	2	36
J.A. Emanuel	7	-	-	7
S. Policastro	56	-	-	56
R.J. Golden	12	5	3	20
W. Kern	16	16	20	52
D.M. Baugher	40	97	7	144
F.W. Wehrfritz	18	36	76	130
A. Warren	160	168	160	488
B. Walmsley	12	16	10	38
Total Engineers	872	910	838	2620
		TECHNICIANS		
Manufacturing Services	1013	1057	1012	3082
Testing Services	593	513	557	1663
Total Technicians	1606	1570	1569	4745
TOTAL	2478	2480	2407	7365

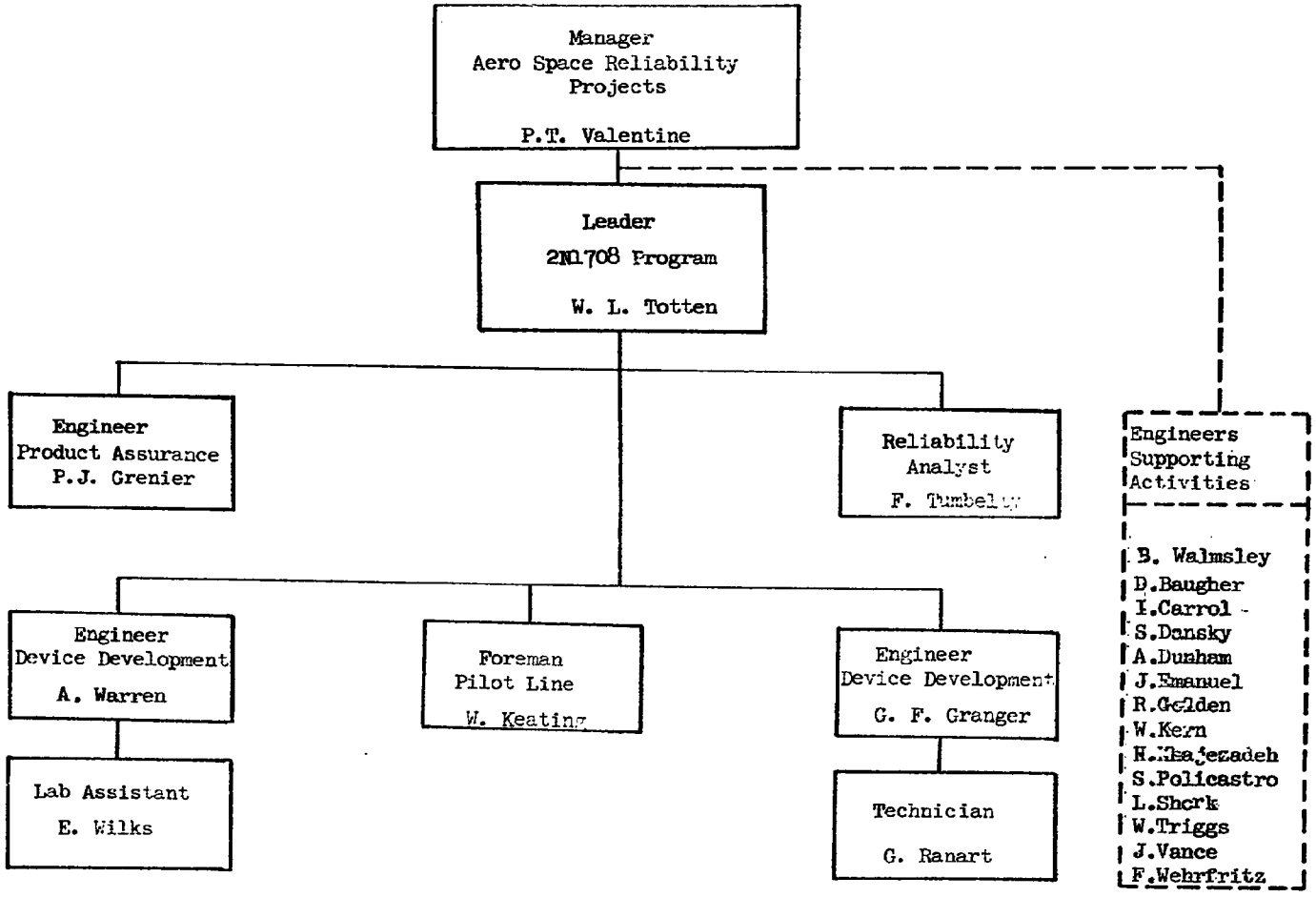


FIGURE 21 2N1708 RELIABILITY IMPROVEMENT PROJECT ORGANIZATION CHART